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Triple-Layer T-Gate Process

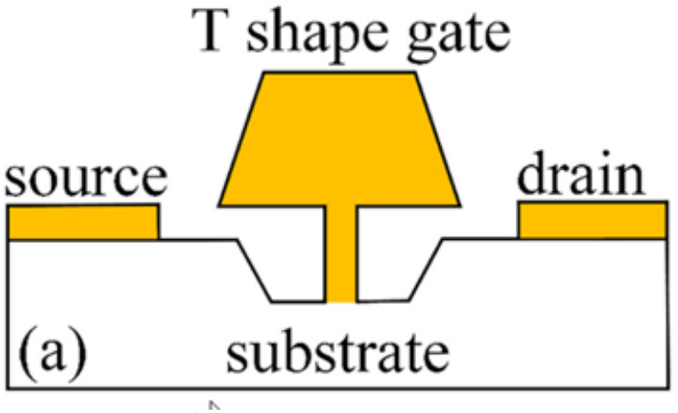
3D E-Beam T-Gate PEC & Wafer Fabrication

Something about T-Gate

- T-shaped gates is essential for development of high power & high frequency devices
- Substrates: high density III-V materials (GaAs, GaN, InGaAs, InP)
- **Most critical: CD control of the foot (gate length)**
- Less critical: wing dimension control

Head/ Wing: increases the cross-sectional area of the gate, reducing gate resistance

Foot: reduces the gate capacitance, higher frequency



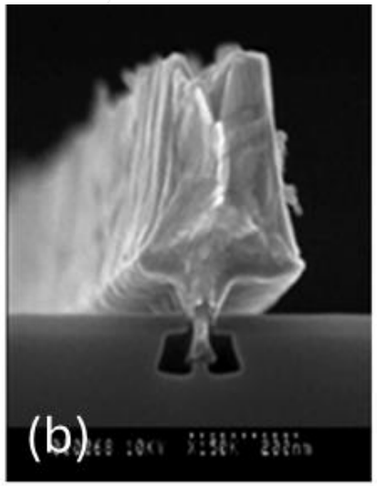
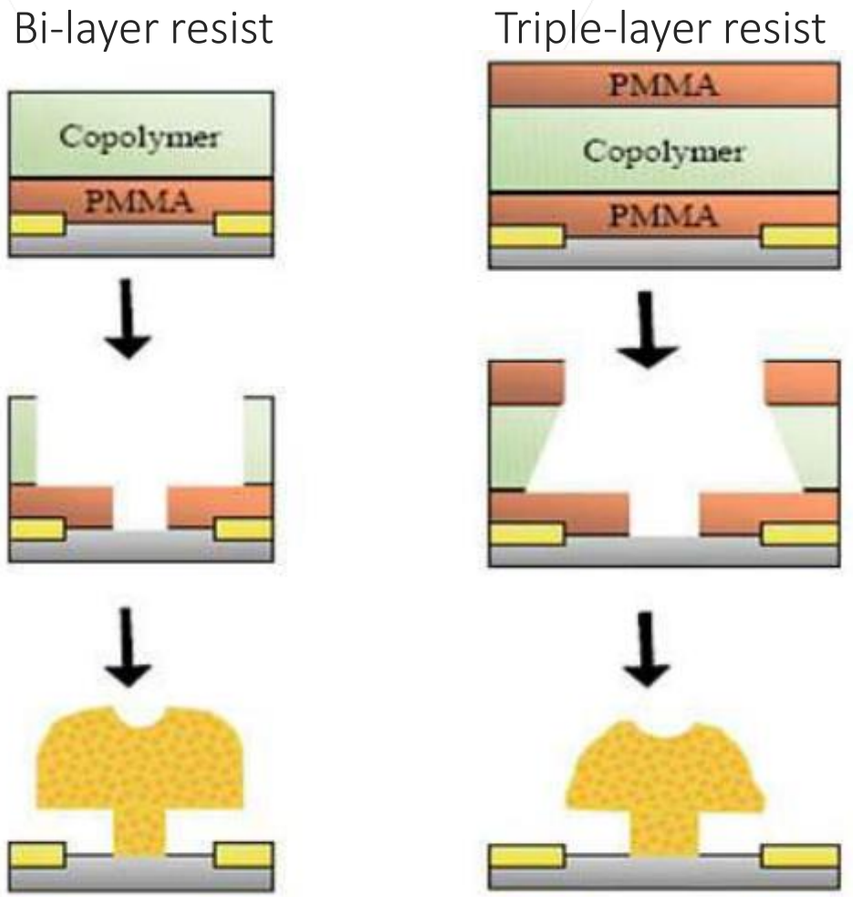


Fig. 1: (a) Schematic cross section view, and (b) SEM image of a T-Gate (Mingsai Zhu et al, Micro and Nano Engineering, 13 (2021), 100091)

T-Gate fabrication

- Multi-layer process: mostly based on Bi-Layer or Triple-layer resist system
- Fabrication methods:
  - Optical (stepper, deep UV) lithography
  - X-ray lithography
  - E-beam/ optical lithography
  - **E-beam lithography**



Source: Microchem

Traditional T-Gate optimization to achieve the target CD

- Run Design of Experiments (DOE) with varying foot and wing size, dose modulation…
  - Iteratively working nicely but tedious and not very stable as slight process fluctuations lead to great variances…

Foot Design in nm: 18,24,30
Wings Total in nm: 456; 504; 552

BD arbitrary chosen at 800micC/cm2

Dose modulations FOOT:
BD+ 115%; BD+130%; BD+145%;BD+160%

Wings dose: BD-50%

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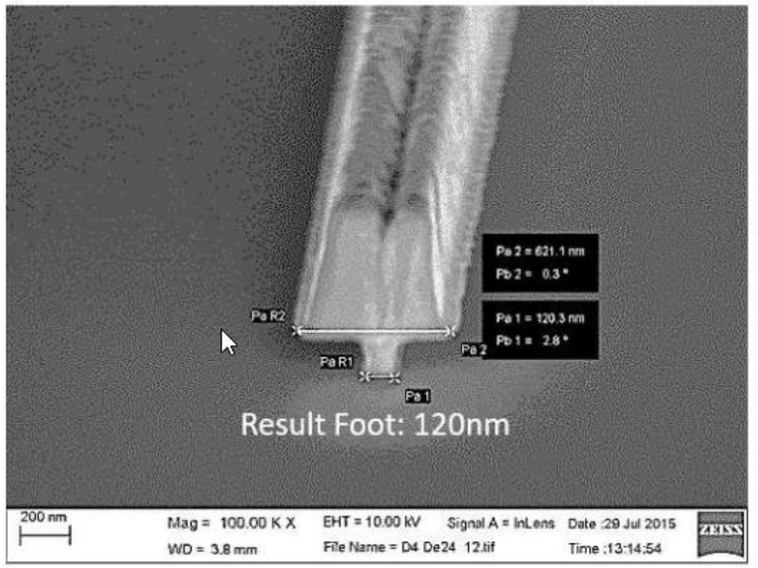


Designed CD foot = 24nm
Result for D4/ CD foot = 120nm

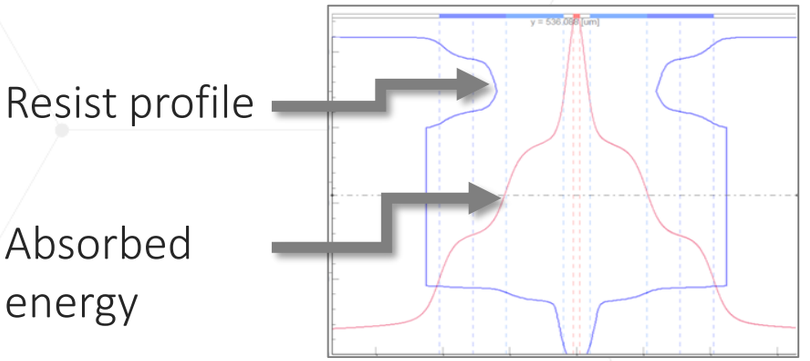
3D E-Beam T-Gate PEC: optimized for multi-layer T-Gate process

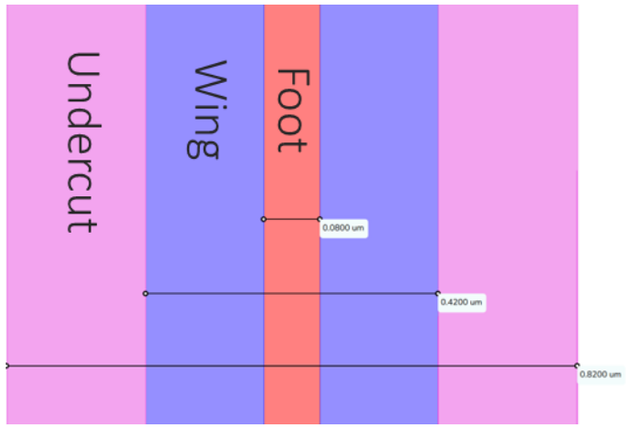
- considering long range proximity effect (PSF)
- considering resist lateral development for foot layer (contrast curve)
- considering the process effect (effective short range blur)
- enables contrast enhancement by using ODUS (Over Dose Under Size) method on the foot layer

Before we start to build T-Gate…

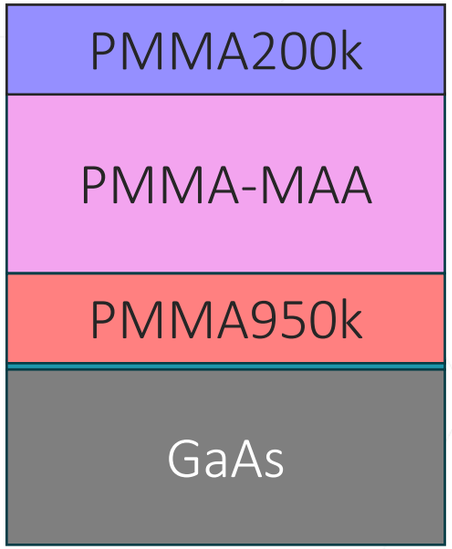
Select suitable resist system by considering:

- Resist compatability (e.g. solvent tolerance)
- Resist sensitivity (contrast curve)

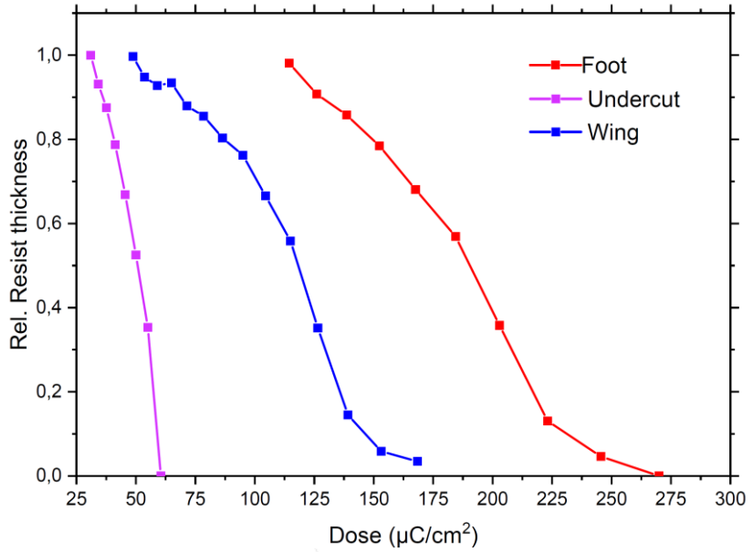




Layout



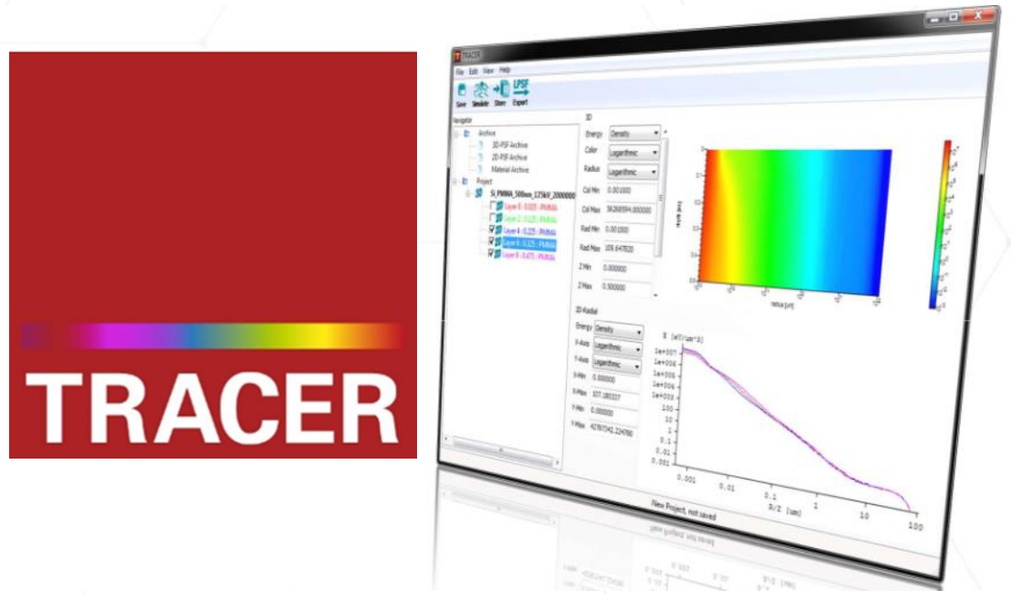
Triple-layer resist system



Contrast curve

Important work before T-Gate PEC:

- Point spread function (PSF): Monte Carlo simulation with TRACER
  - Substrate definition
  - Beam energy, e.g. 50keV, 100keV…
  - Resist stack total thickness
  - Extract the PSF from the foot related depth



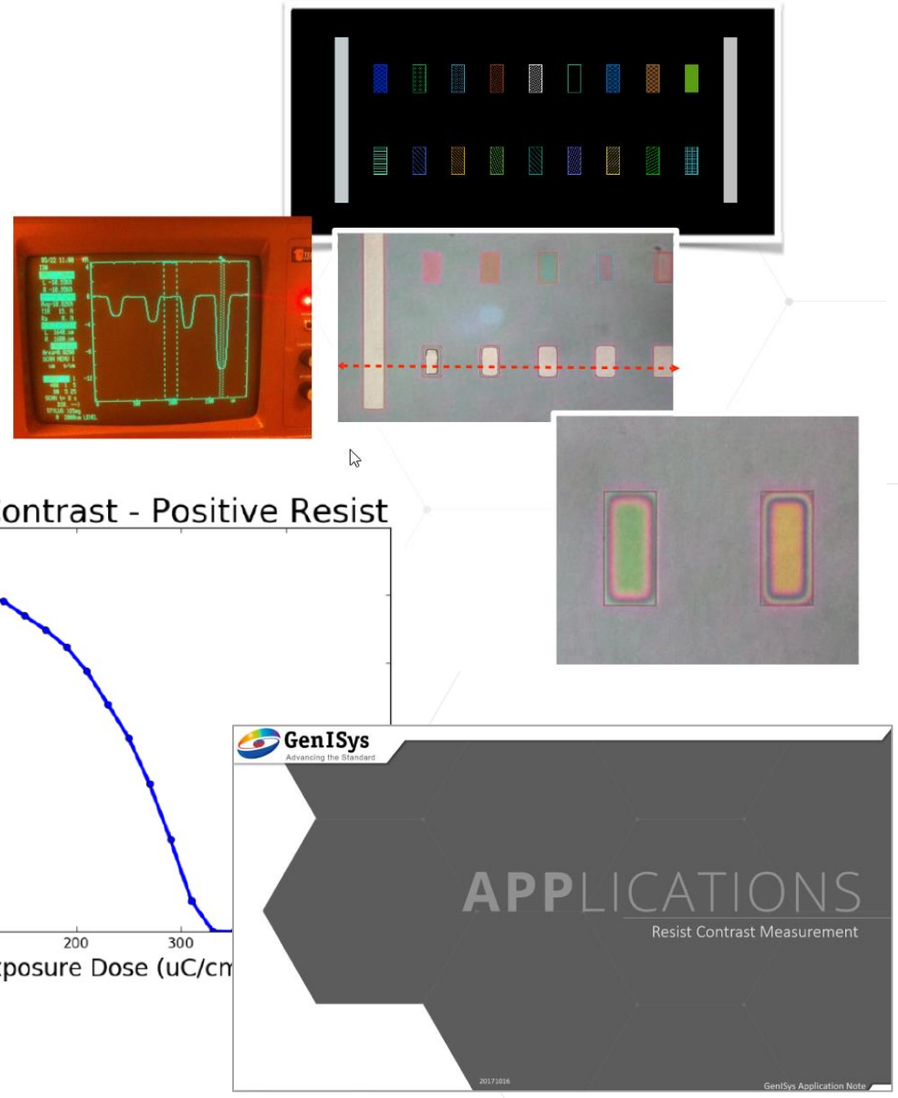
TRACER calculates the absorbed energy spread over resist thickness and distance

Important work before T-Gate PEC:

- Precise contrast curves of each resist layer (wing, undercut, foot) is the key part of 3D PEC correction
  - Resist layer measured individually
  - Pattern
    - Width > 3 x Beta
    - Length easily be measured with profilometer
    - Separated pattern to avoid interaction
    - Typical pattern: 150 µm x 300 µm

Substrate Material	100 kV	50 kV
Silicon	30 µm	10 µm
GaAs	12 µm	4 µm
Sapphire	19 µm	6 µm

Example Beta values

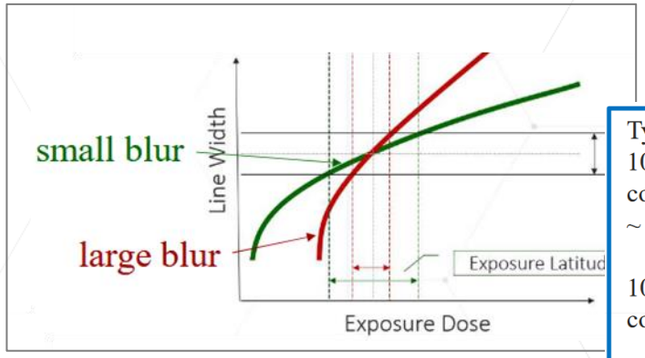


Important work before T-Gate PEC:

- Effective Short Range Blur estimation (Same substrate, resist stack & process parameters)
  - 1st order estimate

$$\text{FWHM} = 0.76 \times \Delta CD \,/\Delta\%dose$$

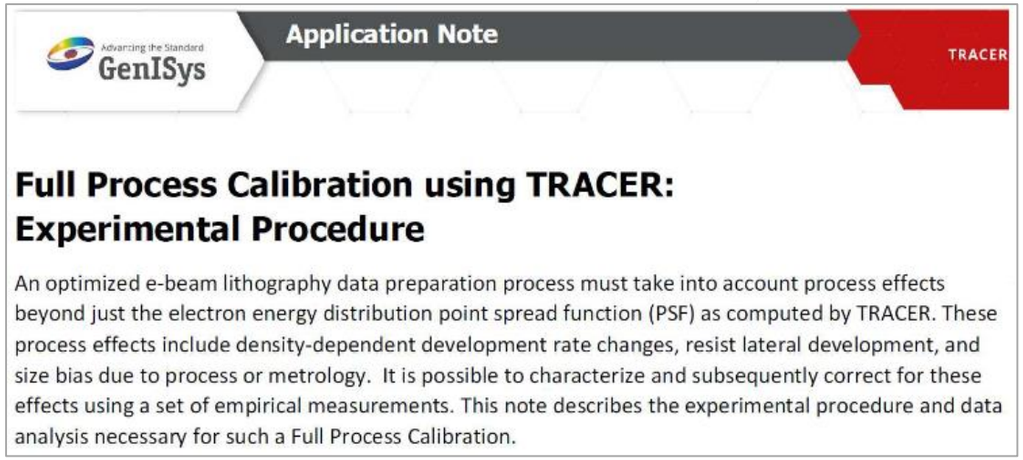
  - Calibrated by TRACER



Typical values:
100keV, low current (~ 1nA), high contrast thin (100nm) PMMA: ~ 15nm

100keV, high current (~20nA), low contrast thick PMMA: ~ 30nm

50keV, high current (~50nA), low contrast thick PMMA: ~ 50nm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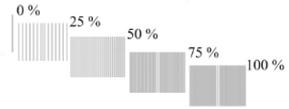
Application Note TRACER

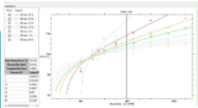
Full Process Calibration using TRACER: Experimental Procedure

An optimized e-beam lithography data preparation process must take into account process effects beyond just the electron energy distribution point spread function (PSF) as computed by TRACER. These process effects include density-dependent development rate changes, resist lateral development, and size bias due to process or metrology. It is possible to characterize and subsequently correct for these effects using a set of empirical measurements. This note describes the experimental procedure and data analysis necessary for such a Full Process Calibration.

Expose Dose Matrix, Process, & Measure Calibration Pattern

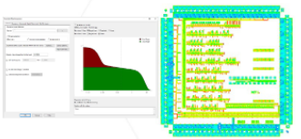


Use TRACER to fit the data and determine correction parameters



- Base Dose
- Effective Process Blur
- Constant and density-dependent bias
- UC/OC Mix Factor

Apply correction parameters using BEAMER's PEC module

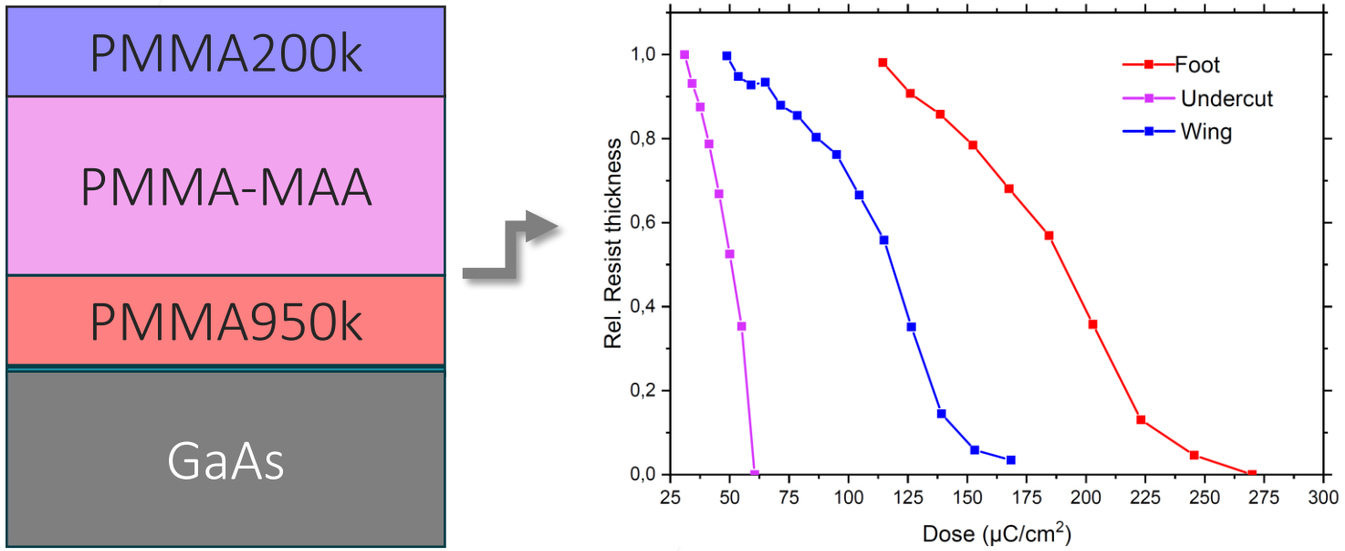


Typical TRACER calibration procedure

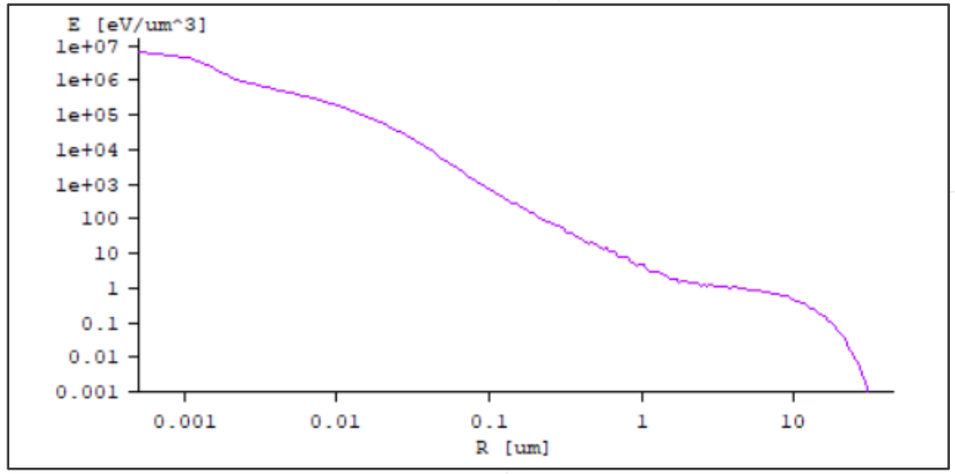
3D E-Beam T-Gate PEC for triple-layer system

BEAMER

TRACER



(PMMA 200k/PMMA-MAA/PMMA 950k)/Si3N4/GaAs



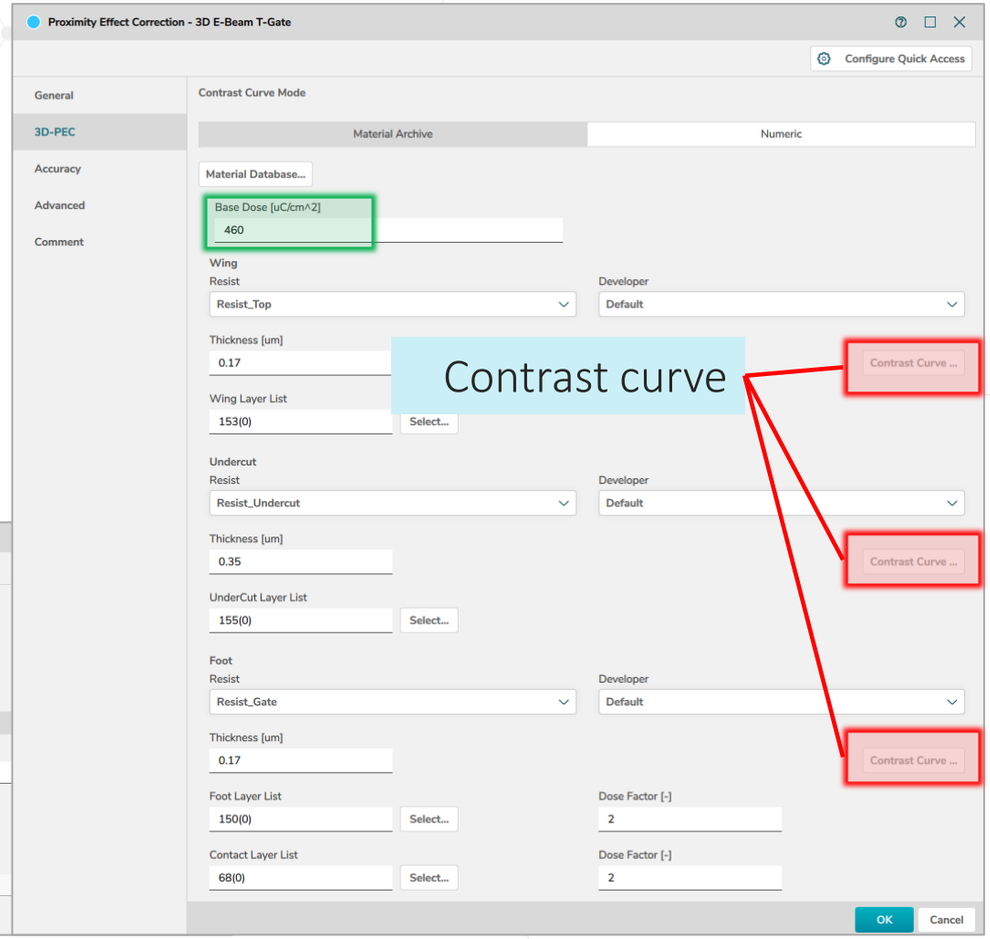
PSF from TRACER

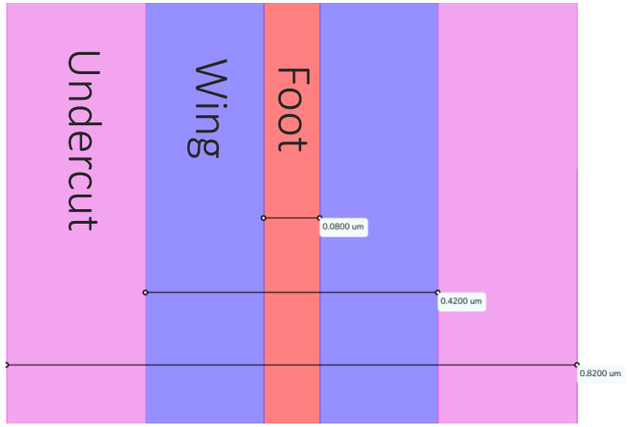
3D E-Beam T-Gate PEC

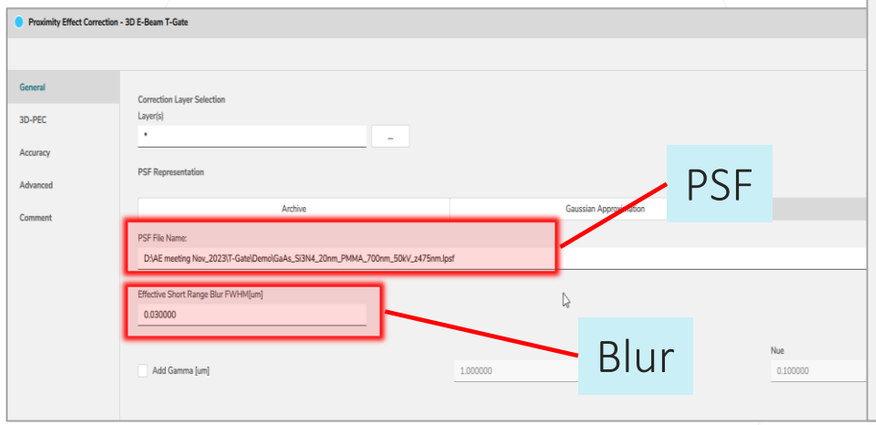
3D T-Gate PEC with following input:

- Contrast curve of wing, undercut and foot layer
- PSF according to the foot depth
- Effective short range blur

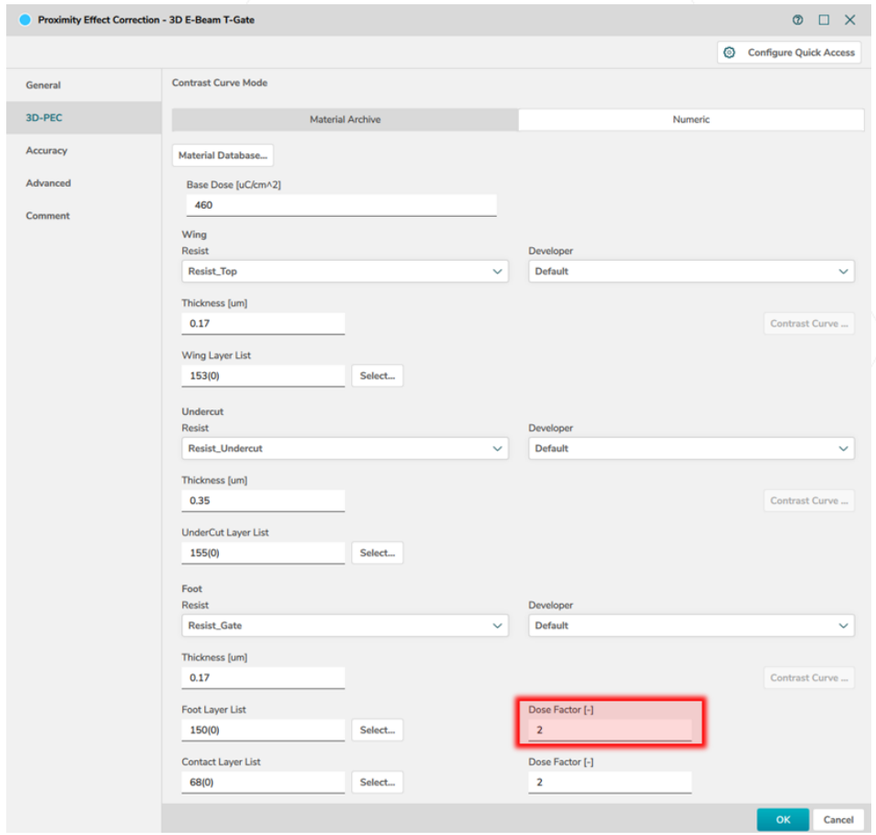
GUI interface

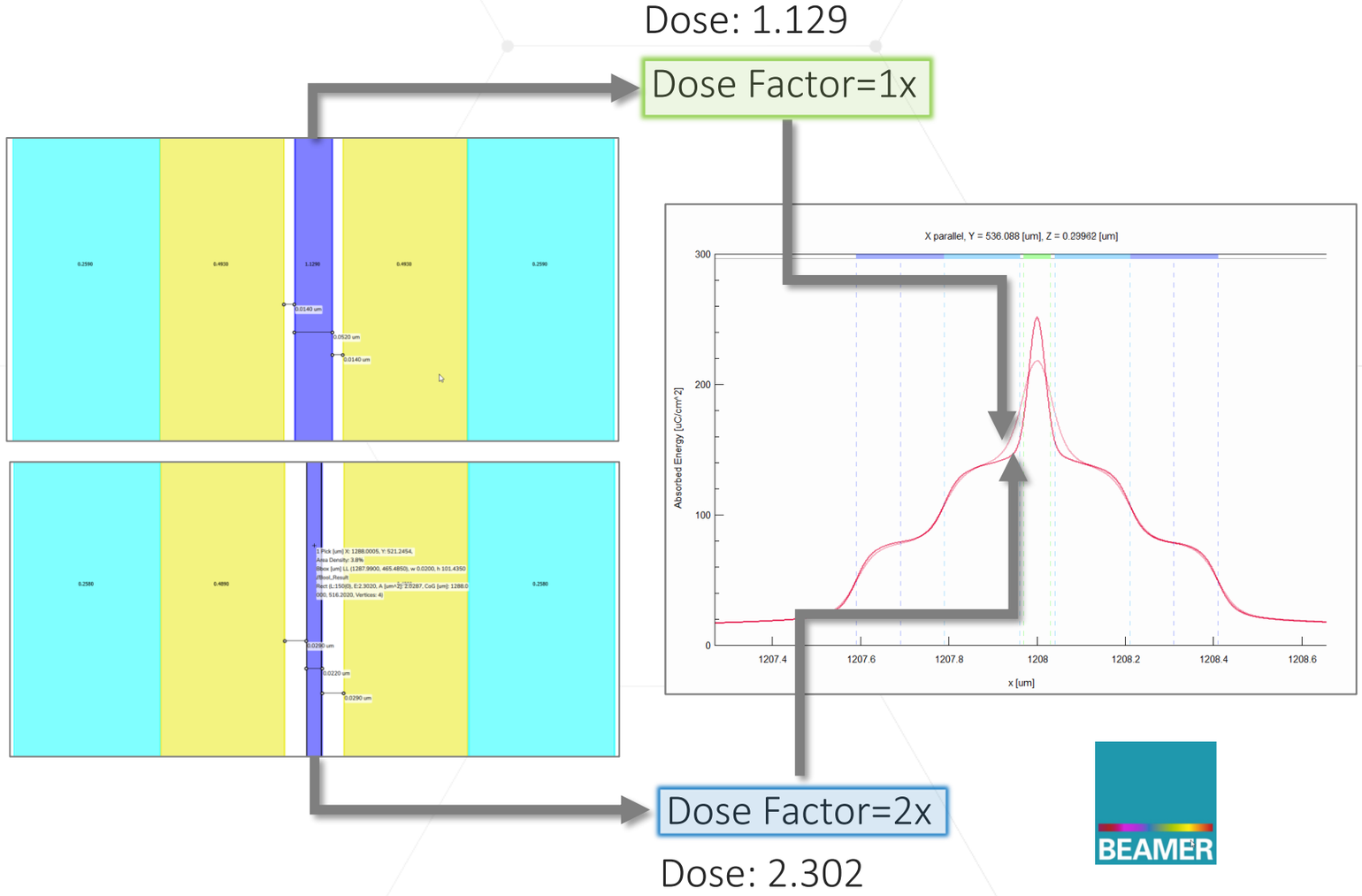






- Dose Factor settings for foot layer

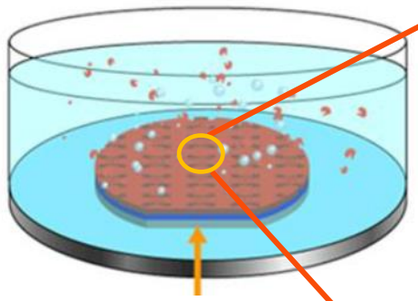




Development simulation with LAB

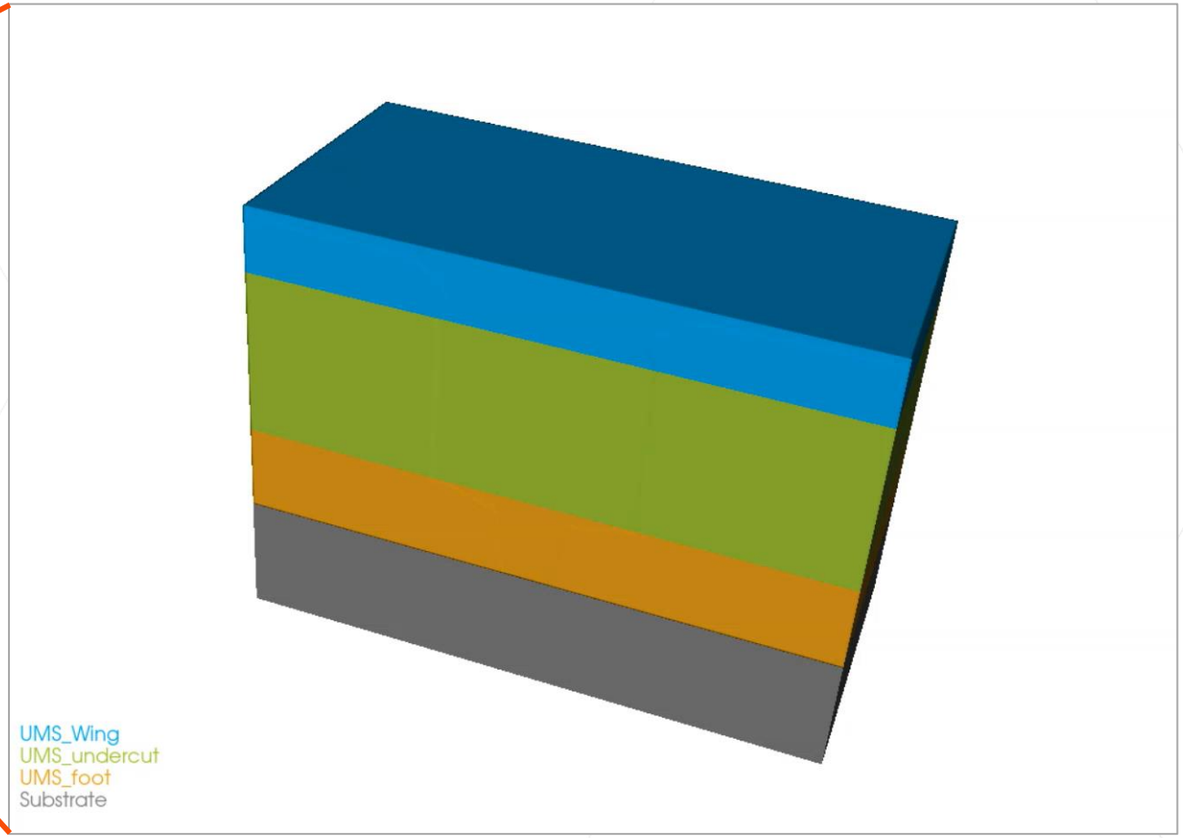
Build T-gate with Tri-layer resist system with single development process

*Development process



Substrate

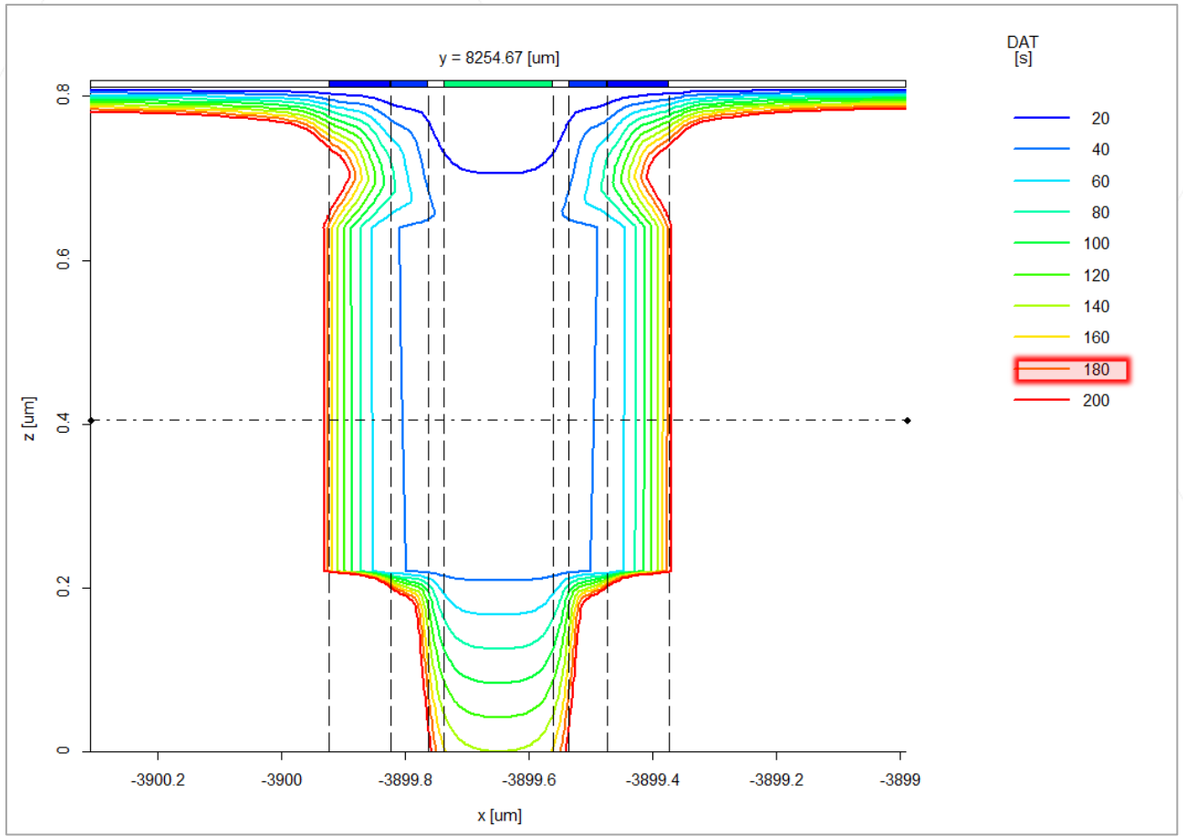
*Image:
https://nanoscale.unl.edu/pdf/Photolithography_Participant_Guide.pdf

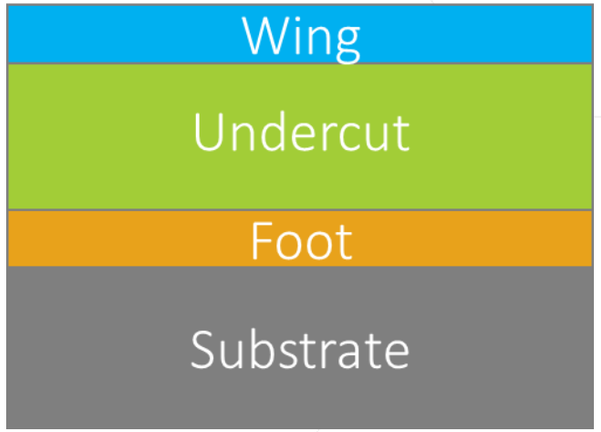


IMPORT
E-Beam 3D
Resist

LAB

Stable T-Gate process suitable for production (Dose Factor=2x)





Developement front movement according to development time

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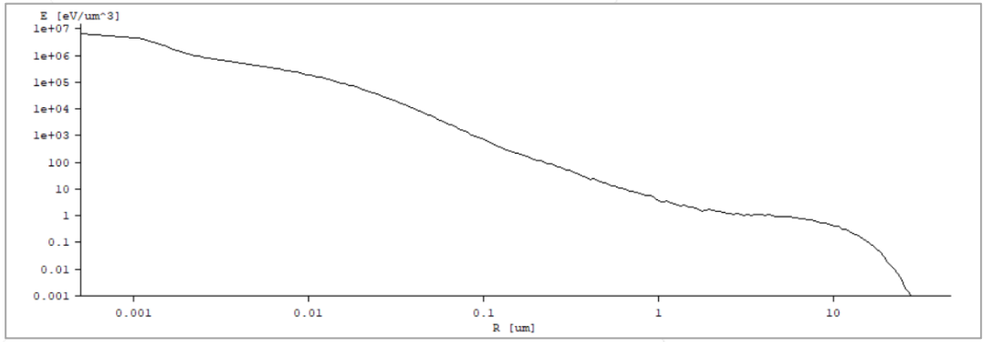
What UMS wants to achieve:

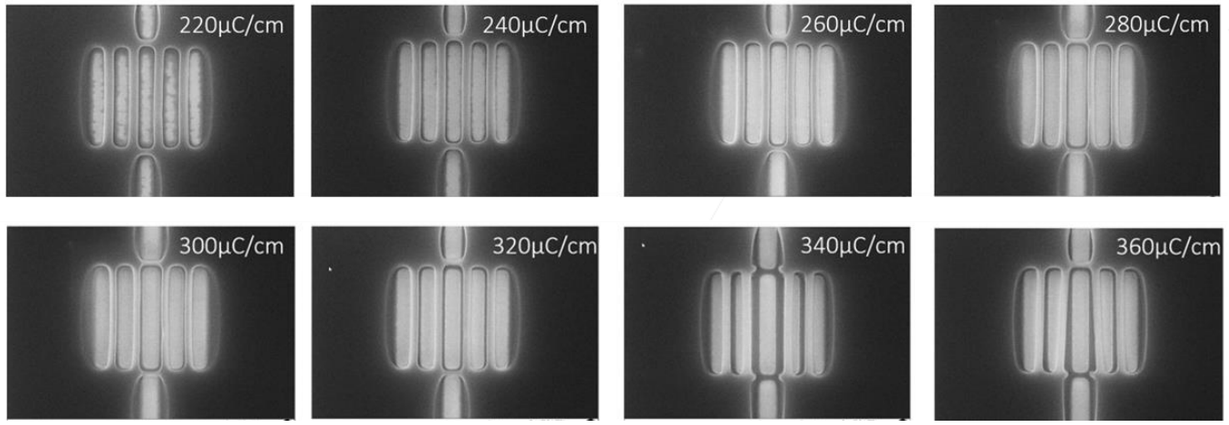
- 100 keV full wafer process
- Substrate: III/V material
- Triple-layer resist system
- One time exposure
- One time puddle development
- Multiple gate length on one wafer (min Gate-length < 100 nm)
- Short exposure time
- Stable process for industry production

Preparation essential parameters for T-Gate PEC:

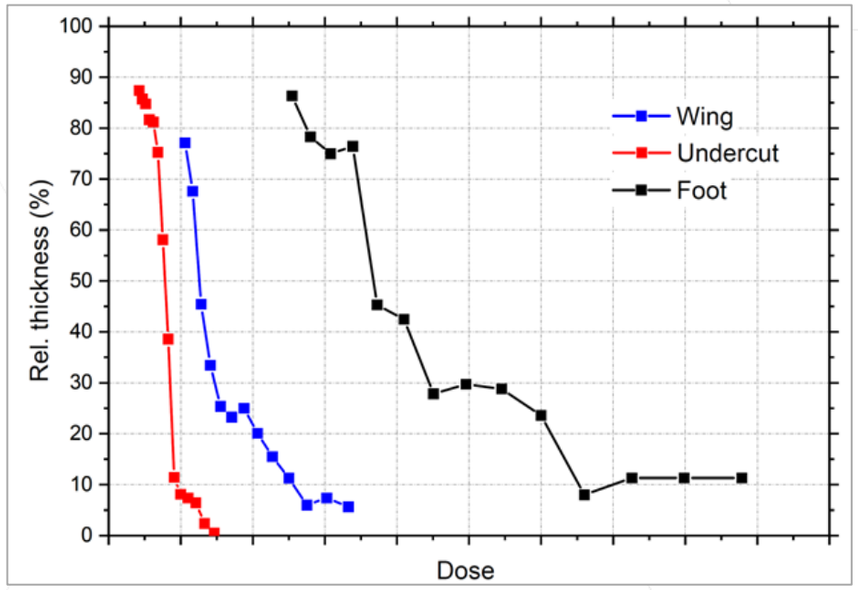
- Contrast curve measurement
- Effective short range blur calibration
- PSF simulation with TRACER



PSF achieved by TRACER



Effective short range blur estimation achieved by ProSEM and TRACER



Contrast curve of all resist layer

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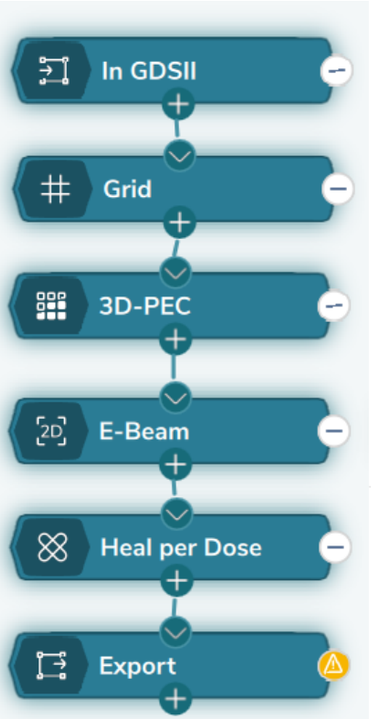
Data preparation for E-Beam exposure:

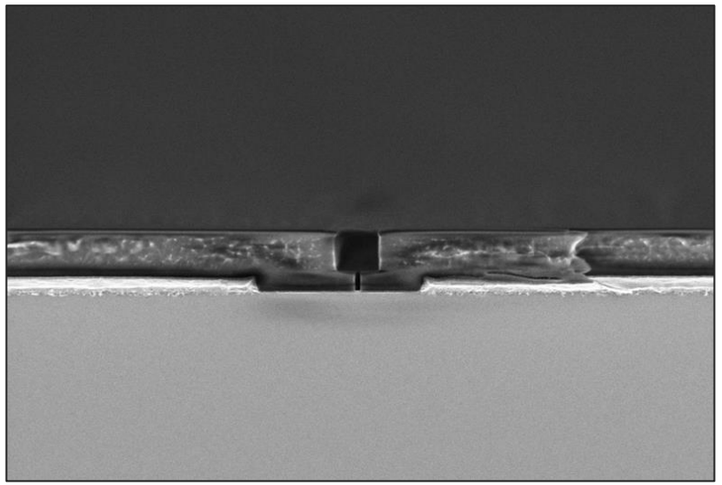
- Layout preparation
- Flow preparation with 3D E-Beam T-Gate PEC

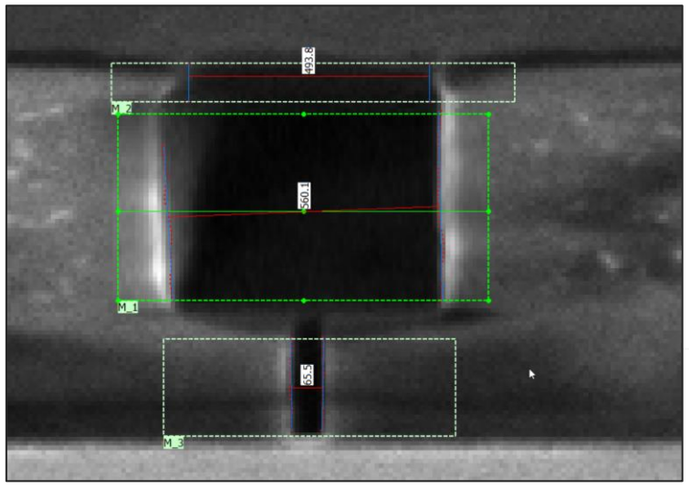


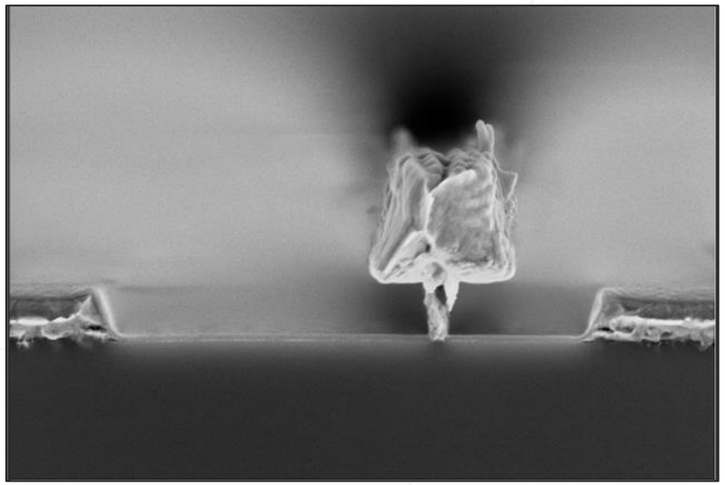
1st test exposure …

1st test exposure

- One time exposure ☺
- One time puddle developement ☺
- Gate-length < 100nm ☺
- Short exposure time ☺







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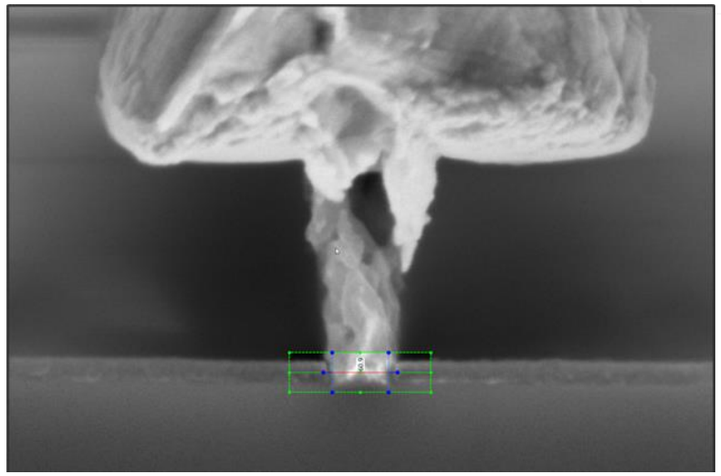
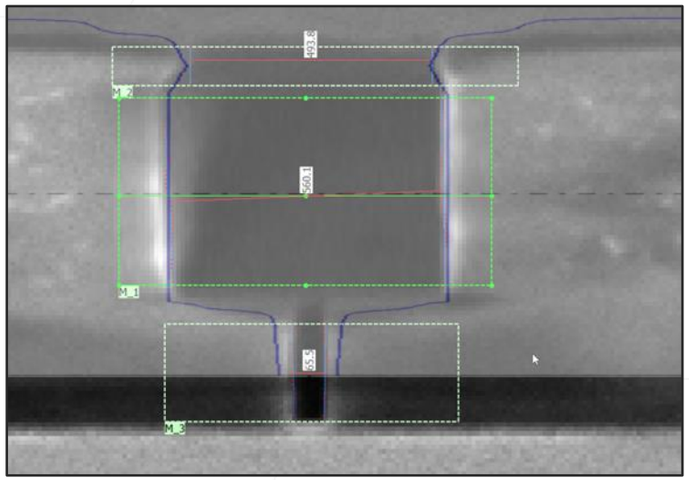
1st test exposure with 100kV after liftoff process

- Problems
  - Gate length CD deviation (e.g. 80nm Gate length: after process is about 60nm)
  - Wing CD deviation (wing oversized)





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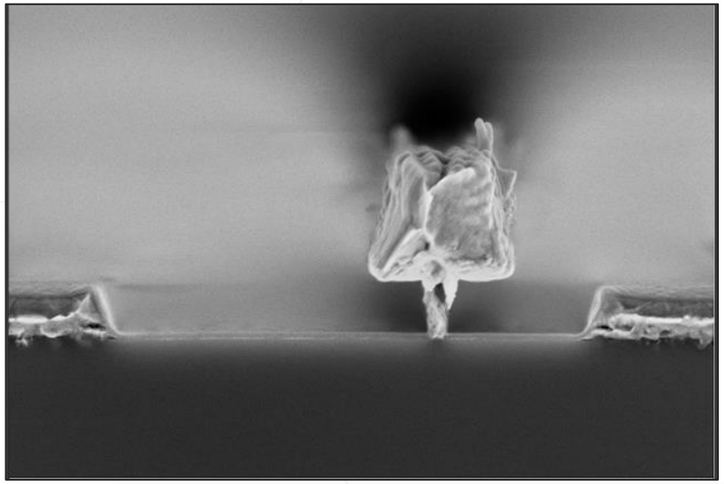
Trouble shooting

- Reason and solution for gate length CD deviation
  - Reason: foot resist layer thickness is thicker due to the existing pre-processed metal patterns
  - Solution:
    - PSF update: New Monte Carlo Simulation (TRACER)
    - 3D T-Gate PEC actulization (BEAMER)
- Reason and solution for wing oversize
  - Reason: wing lateral development not considered in 3D E-Beam T-Gate PEC
  - Solution:
    - Wing CD optimization with application of negative bias (BEAMER)



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After optimization …

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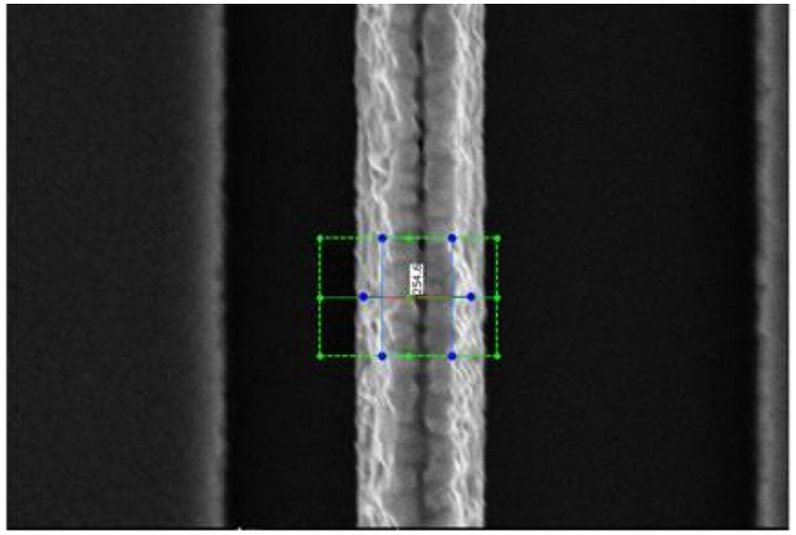
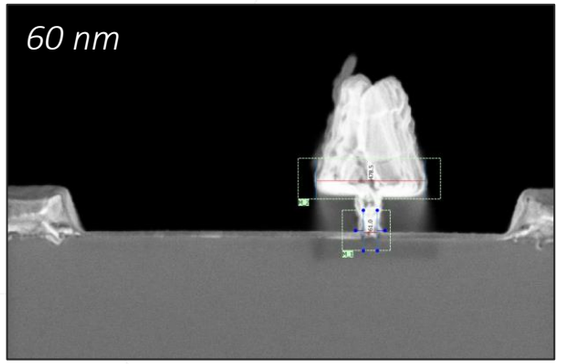
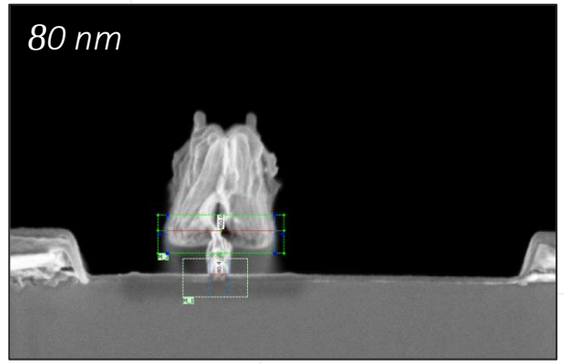
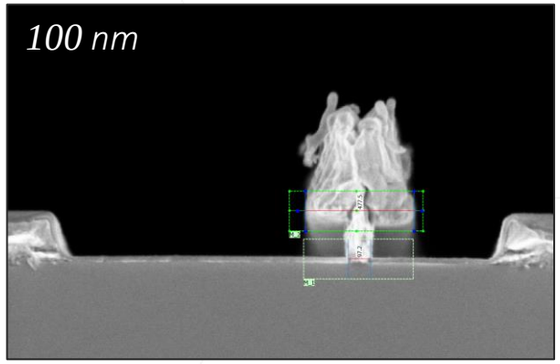
Results after the optimization

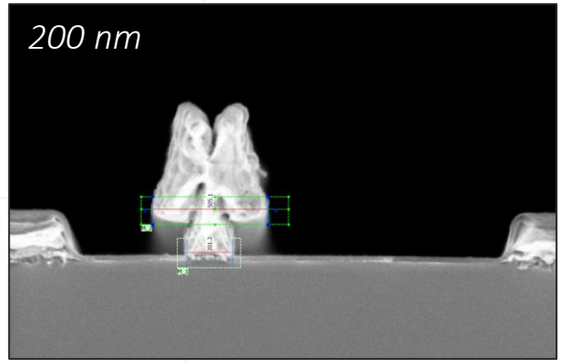
- Gate length CD: on target
- Wing CD: on target
- Stable whole wafer process











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UMS wishes

Fabrication T-Gate with :

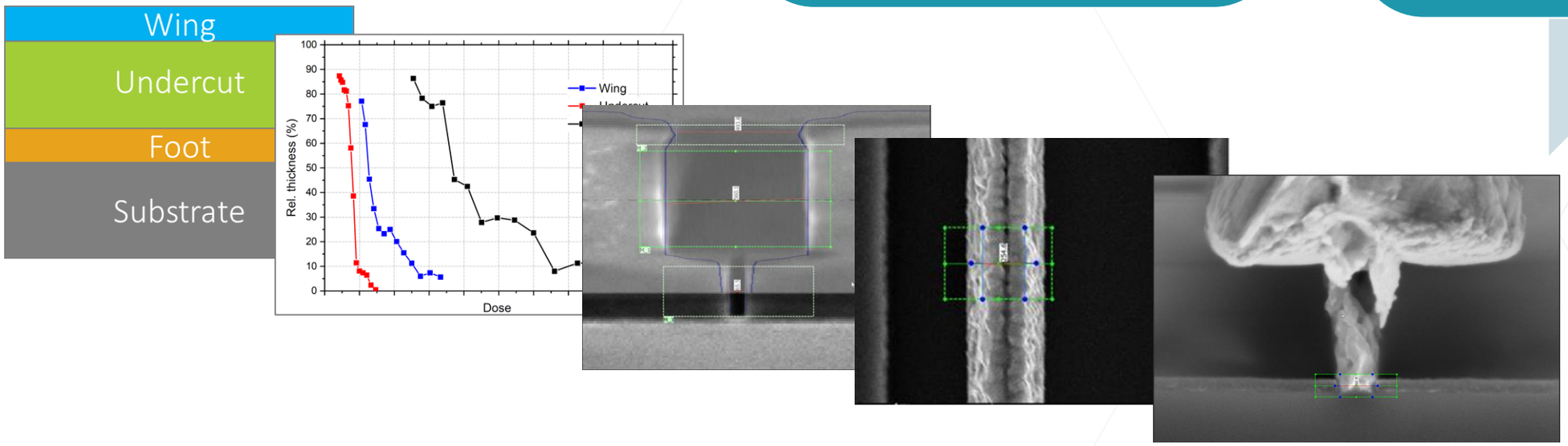
1. One time e-beam exposure
2. One time puddle development
3. min. Gate-length < 100 nm
4. Short exposure time
5. Stable process for production

GenISys offers

1. Help UMS selecting resist stack based on contrast curve analysis
2. Obtaining process Blur
3. Flow preparation based on T-Gate PEC
4. Process optimization

UMS achieves

1. One time e-beam exposure
2. One time puddle development
3. Min. Gate length (60nm) < 100 nm
4. Gate and wing CD on target
5. Short exposure time
6. Stable process for production



BEAMER LAB TRACER Pro SEM

Thank You!

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