Development of sub-100 nm T-Gate for industry application

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Offen im Denken

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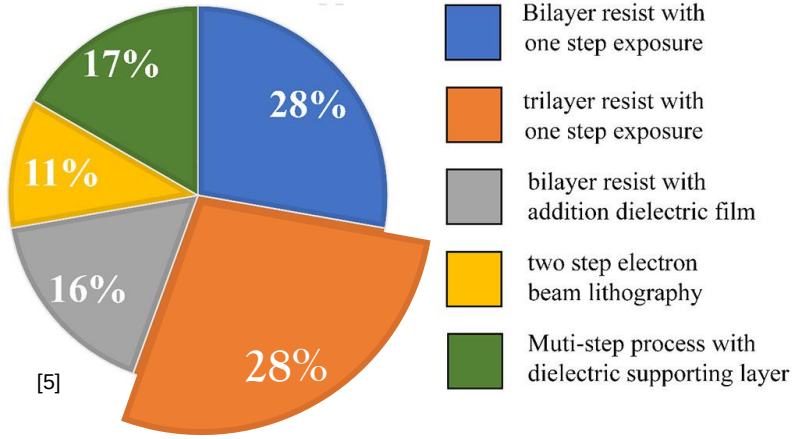
T-Gate State-of-the-art

- Multitude of techniques to reach small foot lengths
- Variation in Layer stack, exposure step amount and usage of dielectric films
- Single step exposures simplicity provides a good base for robust processes
- Two step exposure delivers better length control for the cost of complexity
- Smallest feature sizes with multi step exposure and support by dielectrics

Single step exposure with small gate lengths and high beam current for industry purposes

Gate-Length	Layer stack	Dielectric film	Specialty	Reference
10 nm	Foot: ZEP520A Wing: PMMA/LOR/UV III	SiNx	Two exposure steps, recessed gate	1
20 nm	PMMA/LOR/UV III	none	Two exposure steps, Bilayer	2
80 nm	Foot: ZEP520A Wing: UV6	none	Two exposure steps, very high aspect ratio	3
50 nm	PMMA/LOR/ CSAR	none	Single step exposure, Trilayer	4



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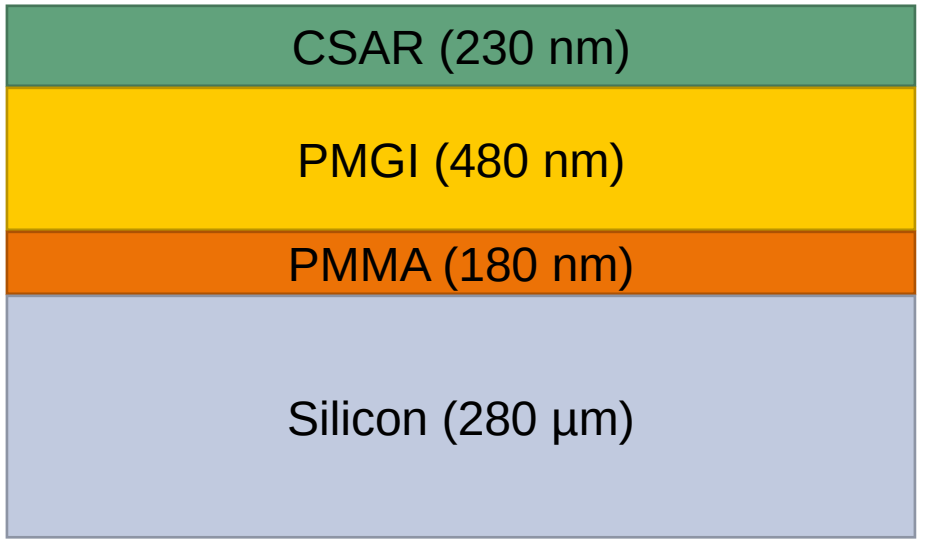
Resist stack

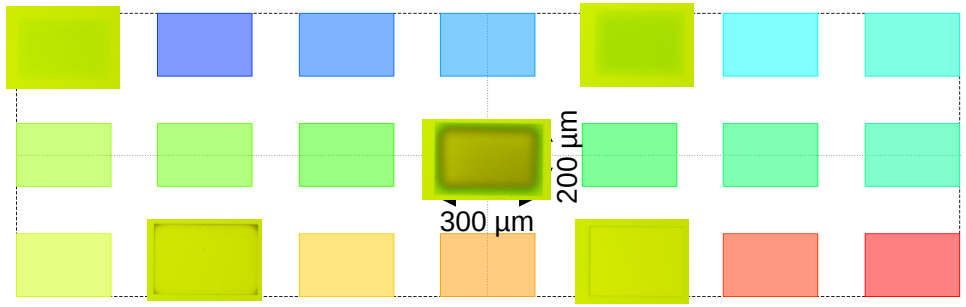
- CSAR62 has low D2C and with high resolution
- PMMA950K offers a higher D2C with high resolution
- In combination CSAR62 is used as wing layer with PMMA950K as foot layer
- PMGI is used as a lift-off resist with no electron sensitivity

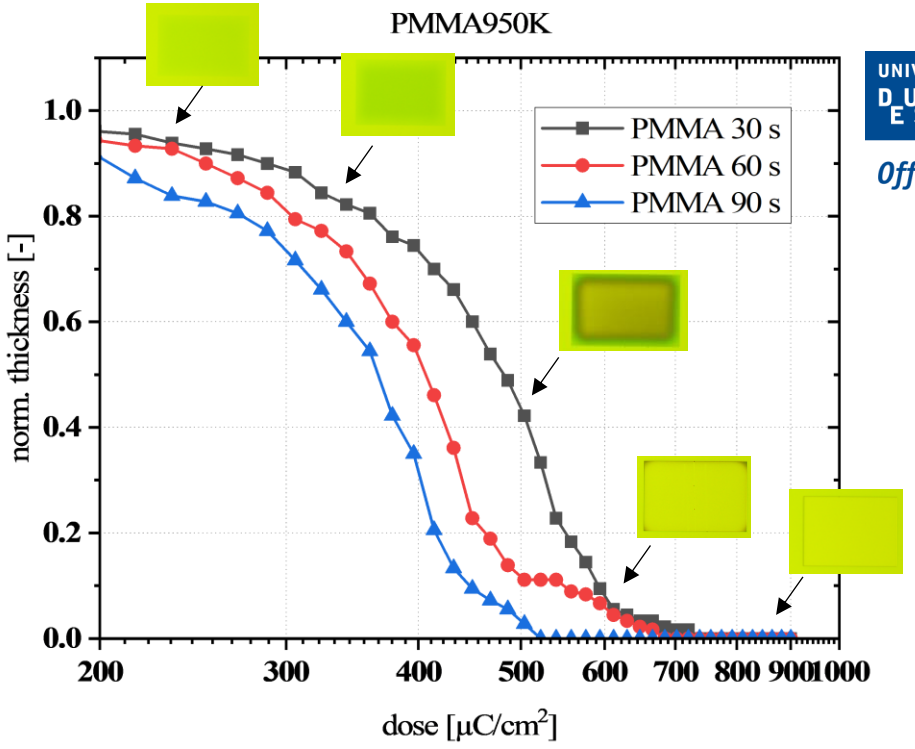


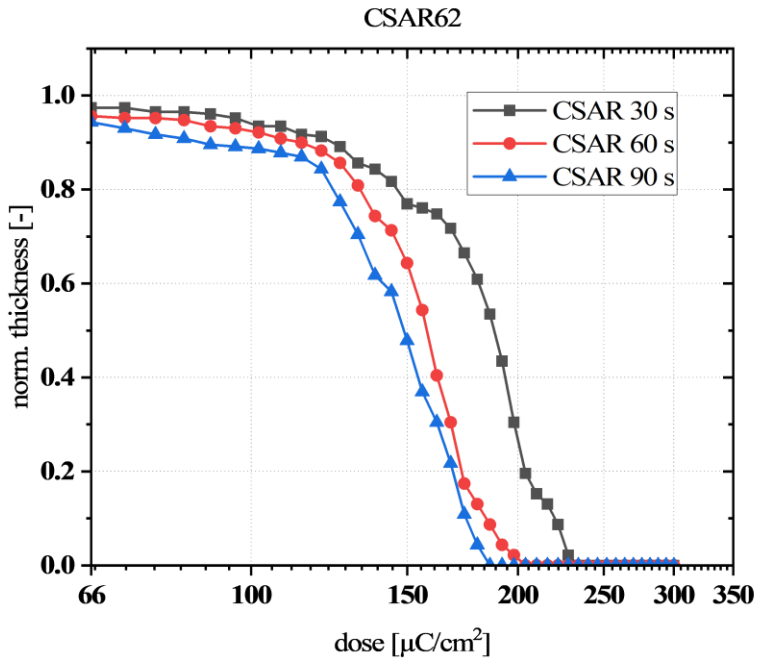
Layer	Resist	Developer
Wing	CSAR62 (AR-P 6200.09)	ZED-N50
Undercut	PMGI.SF8	AZ Developer
Foot	PMMA950K (AR-P 679.03)	MIBK:IPA 1:3

Development and cross-development

- Taking up Contrast curve/dissolution rates of the resists with their respective developers
- Checking cross-development for further process knowledge
- PMMA950K contrast curves deliver D2C of 600, 520 and 470 µC/cm² at 30, 60 and 90 s respectively
- CSAR62 contrast curves show a D2C of 220, 180 and 165 µC/cm² at 30, 60 and 90 s respectively



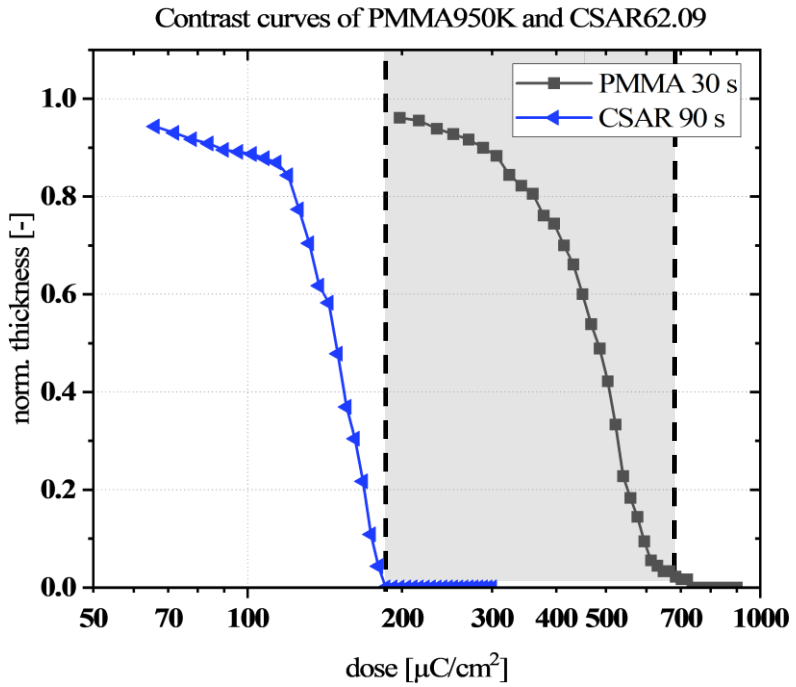


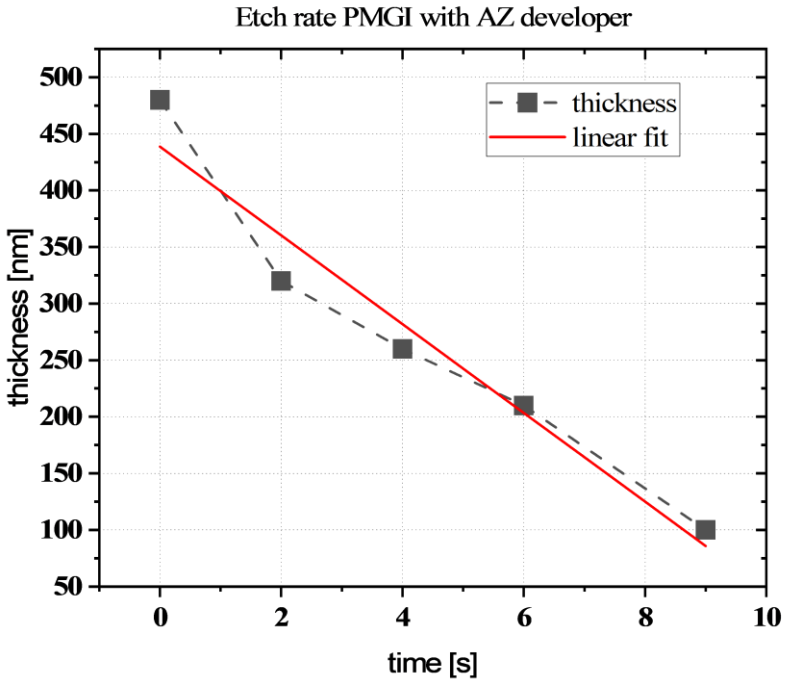


Development and cross-development

- Dose window of 165 – 600 µC/cm^2 for MIBK:IPA 30 s and ZED-N50 90 s
- PMGI measurements provide a dissolution rate of 40 nm/s
- MIBK:IPA 1:3 develops CSAR62 slightly
- ZED-N50 develops 10 nm PMGI in

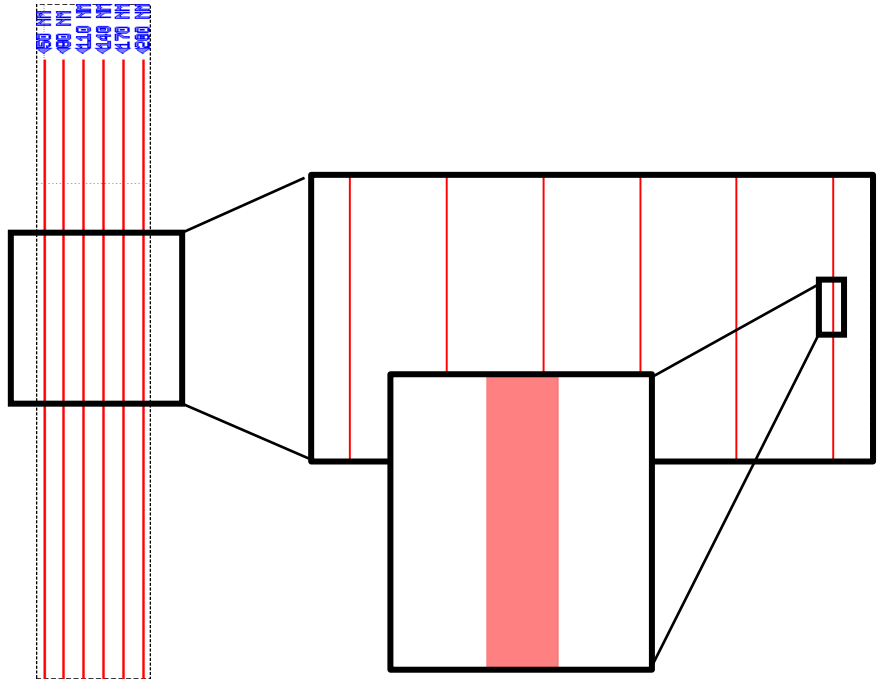
	MIBK:IPA 1:3 30 s	AZ Developer 15 s	ZED-N50 90 s
PMMA950K	+	-	-
PMGI	-	+	-
CSAR62	minimal dissolution < 10 nm	-	+

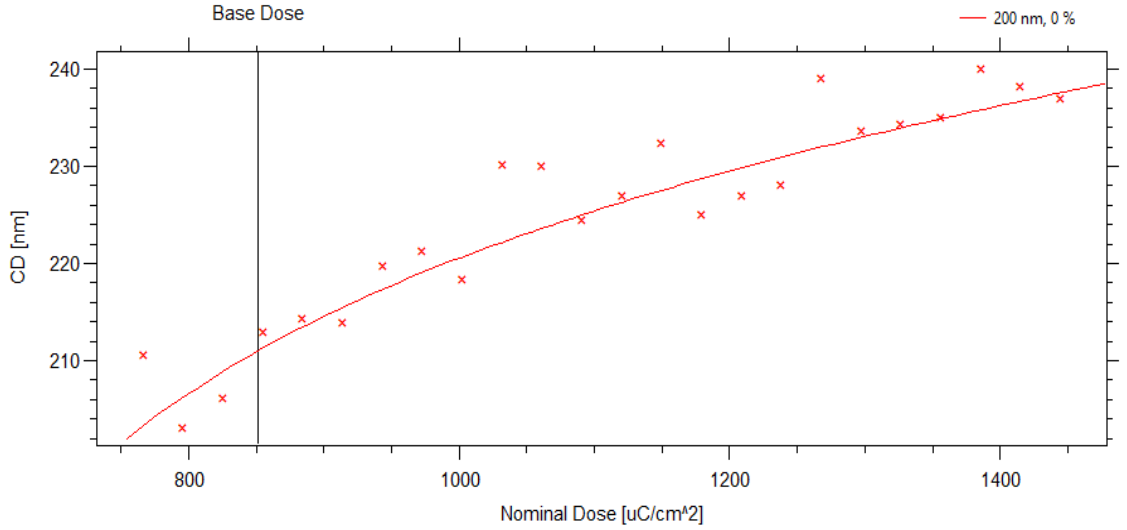




Process calibration for determination of blur

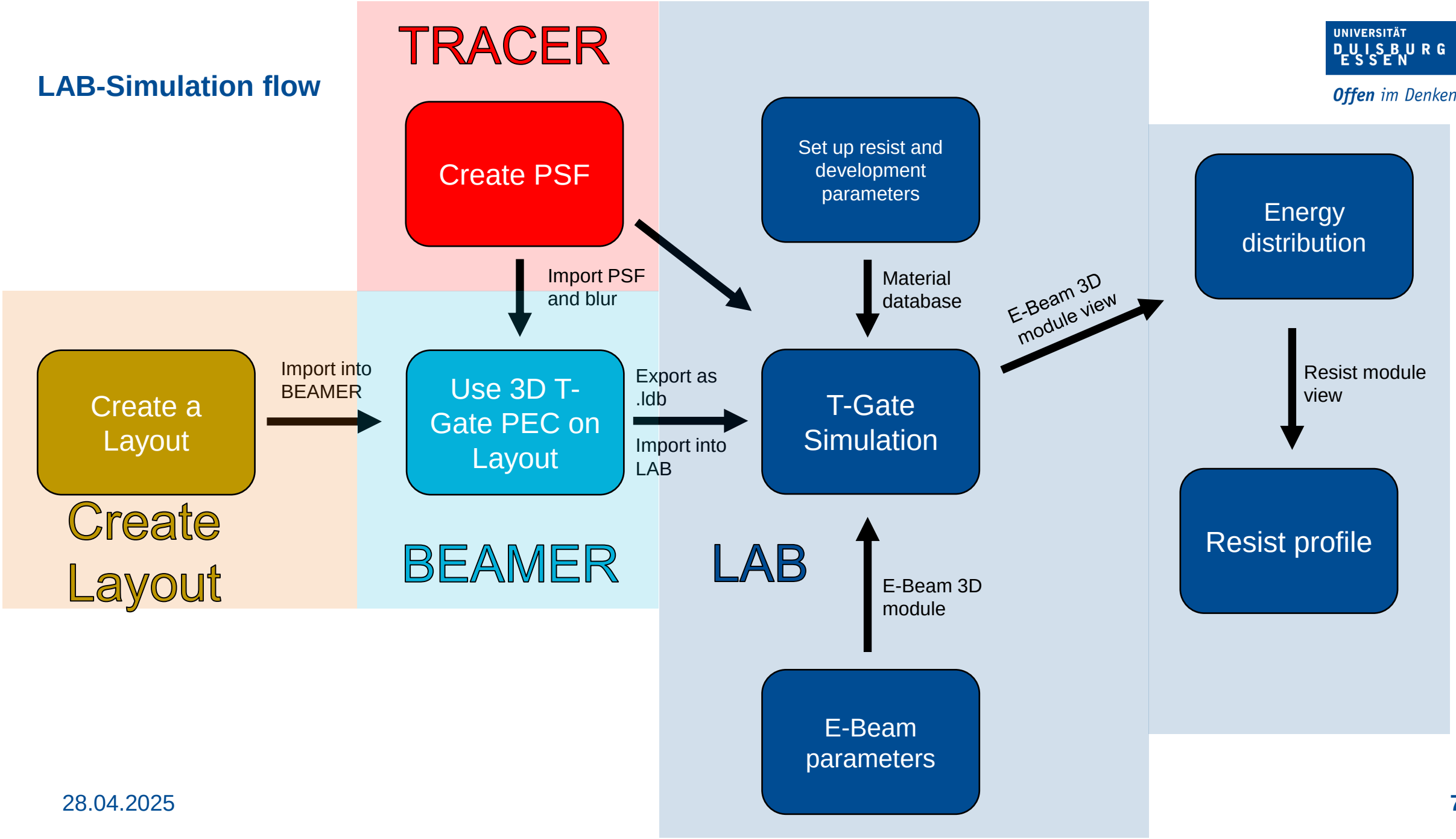
- Process blur influences the deviation of real structure dimensions to target dimensions
- Created by all steps in the process and condition of resists
- Experimentally obtained by a single line measurement at different doses
- Process for whole trilayer with measurement at foot layer
- Measurement took place with ProSEM
- Transcribe Measurements into TRACER to fit
- Blur is found to be 50 nm for this process



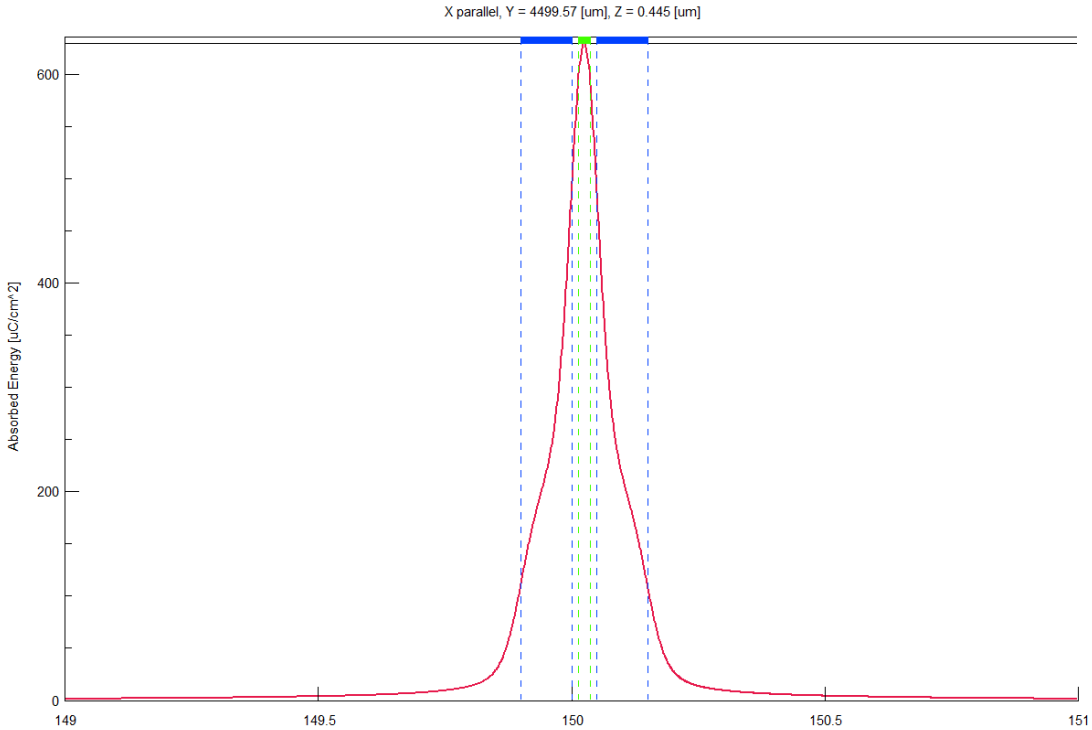


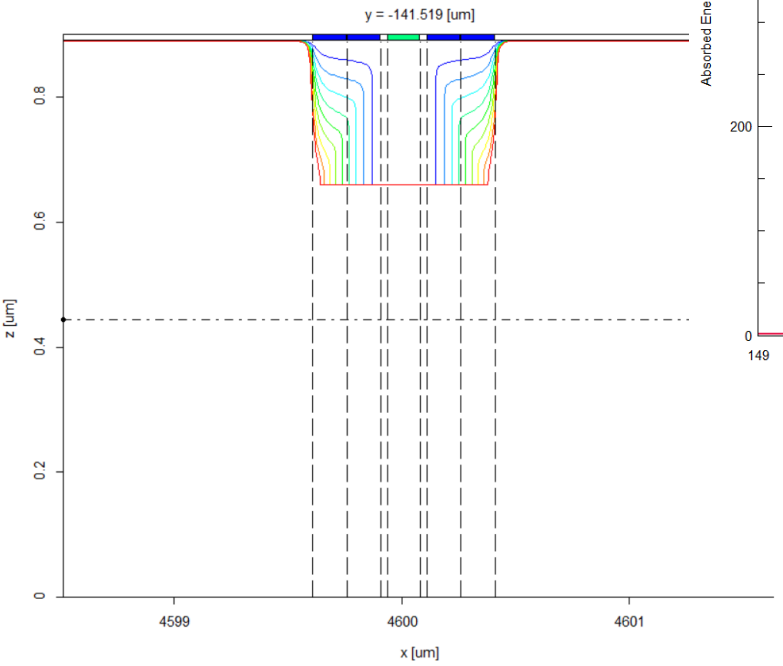
		Optimize?
Base Dose [uC/cm^2]:	851.04	☑
Process Blur [nm]:	51	☑
Additional Mid Range [nm]:	0	☑
Mid Range Weight:	0.00	☑
Constant Bias [nm]:	11	
Contrast [%] / Clearing [%]	100 / 0	
D0 [uC/cm^2]:	630.15	☐
Overdose:	1.00	
Max. Fit Density [%]:	100	
Fit RMSLE [-] / RMSE [nm]	0.047 / 3.474	

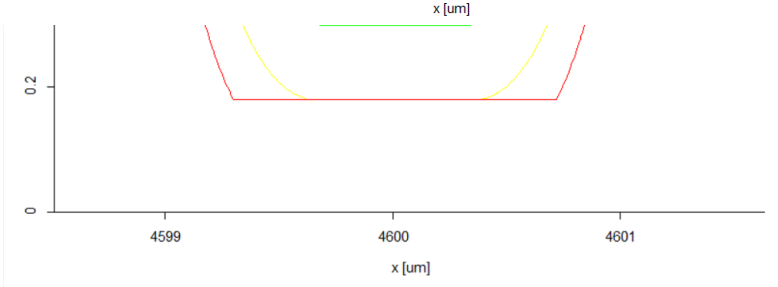
LAB-Simulation flow

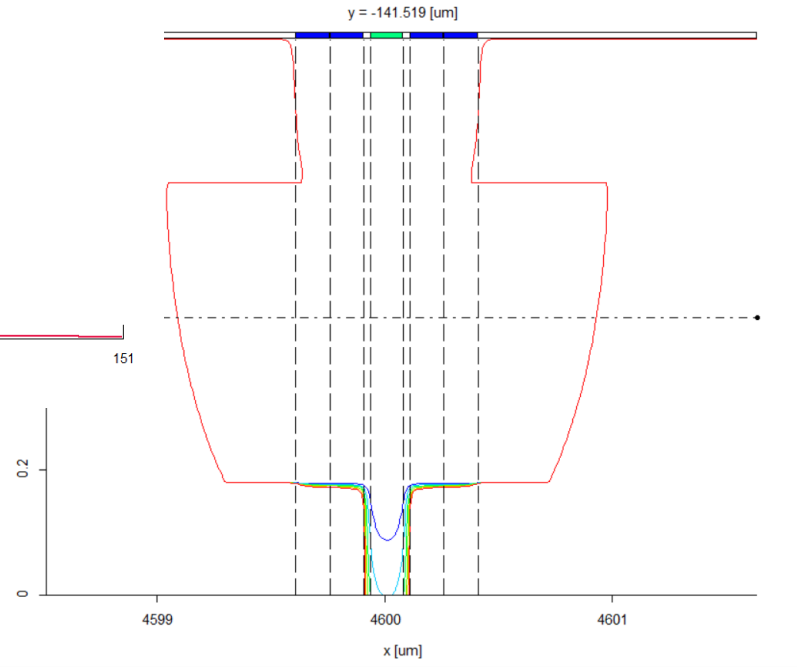


LAB-Simulation



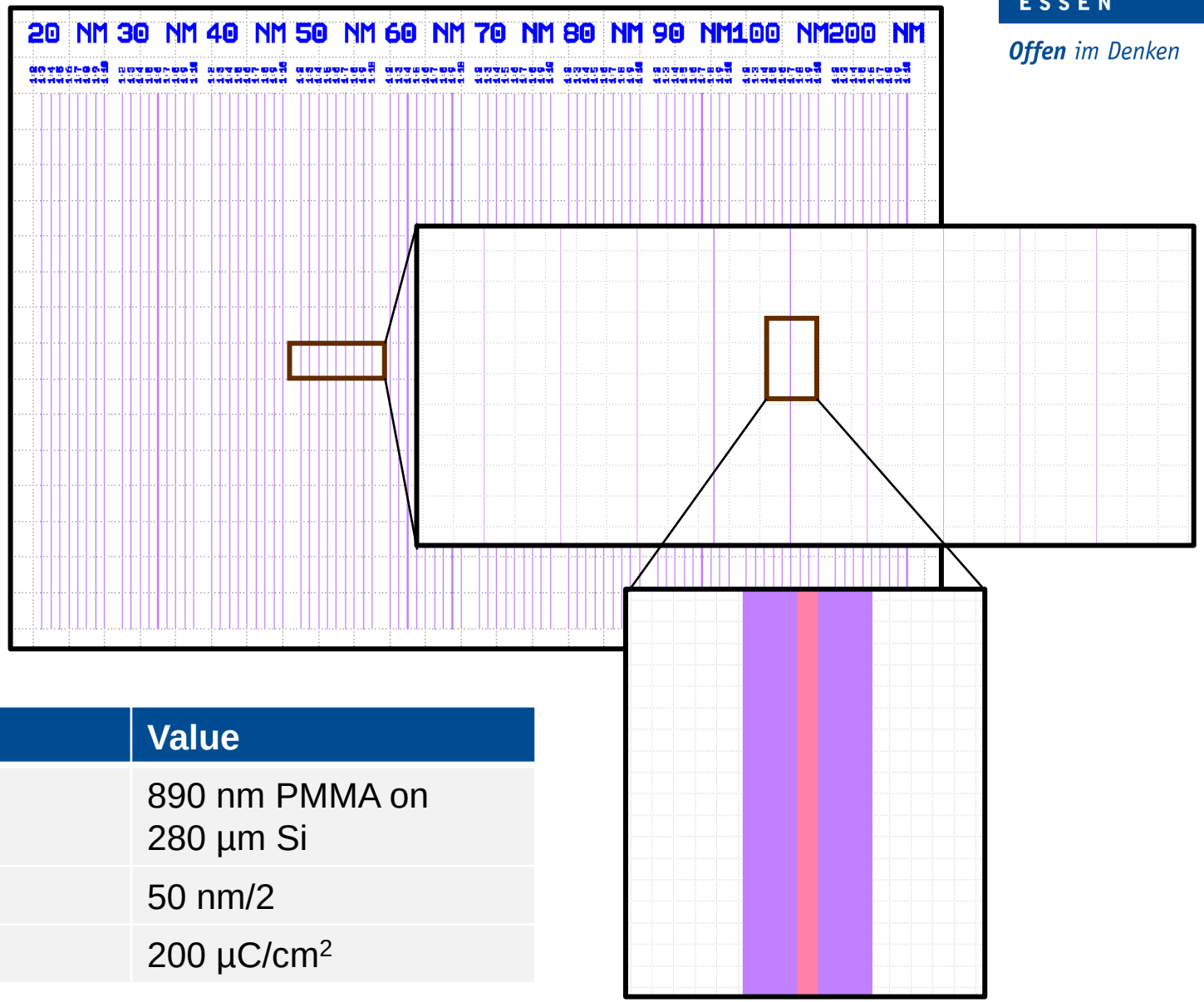






T-Gate Experiment

- Layout consists of multitude of T-Gates
- Two parameters are varied; foot-length and foot/wing ratio
- Layout correction with 3D T-Gate PEC in BEAMER
- PSF for PEC is created with TRACER



Foot/Wing ratio	Foot-length [nm]
1:2, 1:3, ..., 1:10	20, 30, …,100, 200

Parameter	Value
PSF	890 nm PMMA on 280 µm Si
Blur/Dose factor	50 nm/2
Base dose	200 µC/cm^2

T-Gate Experiment

- Spin-coating of the trilayer
- E-Beam exposure in JEOL 8100FS 100kV and 15 nA
- Development of the trilayer
- Lift-off
- Metrology

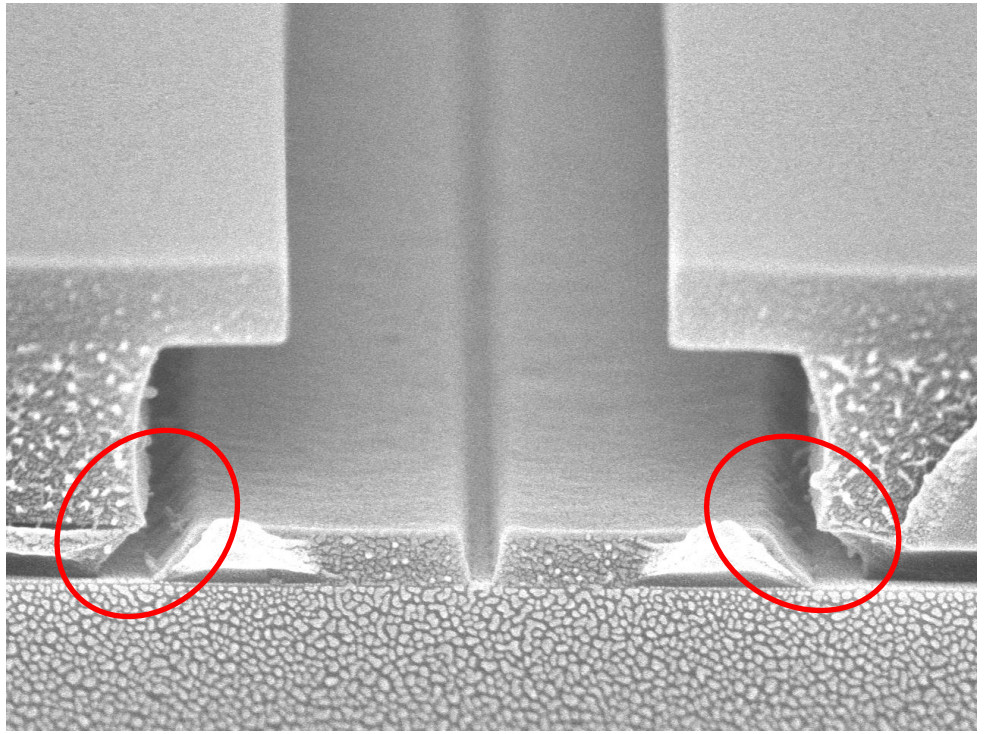
Resist	Acceleration [rpm/sec]	Time [sec]	Rotation speed [rpm]
CSAR62	1000	60	4000
PMGI	1000	60	5000
PMMA950K	1000	60	4000

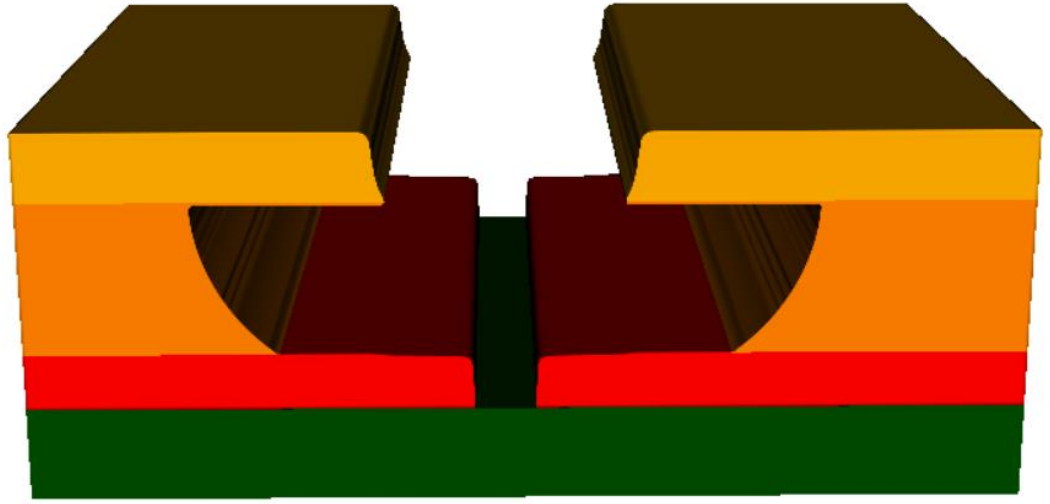
Resist	Developer	Time [sec]	Mixing ratio
CSAR62	ZED-N50/IPA	90/30	Pure
PMGI	AZ Developer/DIW	15/60	Pure
PMMA950K	MIBK:IPA/IPA	30/30	1:3

Parameter	Value
Ashing	O2 50 W 30 sec
PVD	20 nm Ti, 420 nm Au
Lift-off	Acetone

Trilayer resist profile

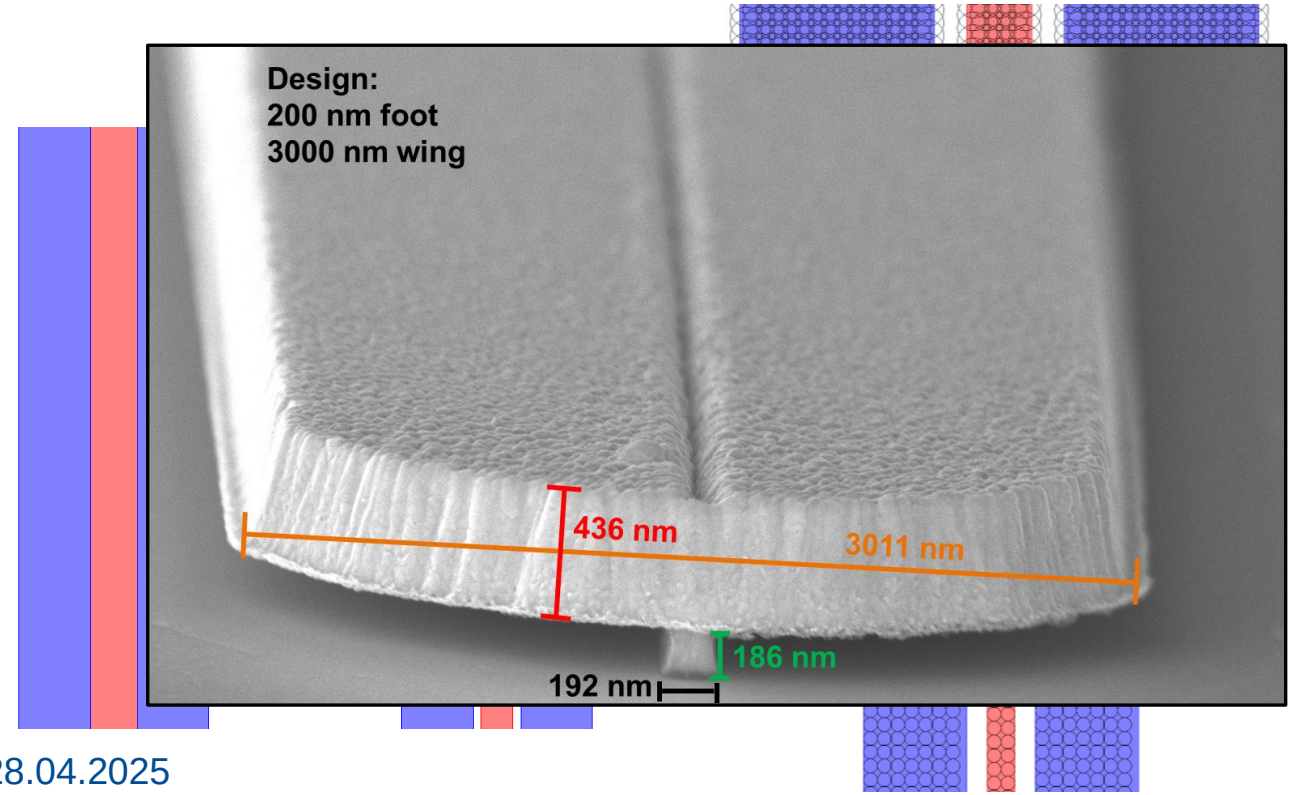
- Comparison of simulation and measured profile shows a lot of similarities
- PMGI layer edges formed differently; no influence on lift-off
- Good prerequisites for successful PVD and lift-off

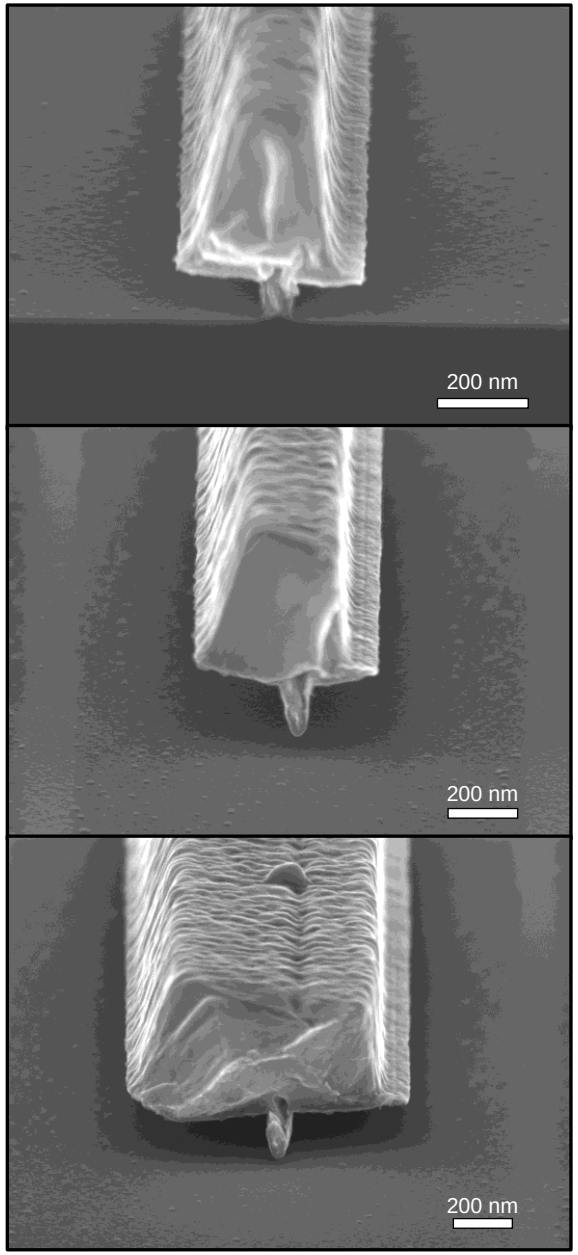




T-Gate

- Multiple writing and correction parameters define the outcome of the T-Gate
- Analysis of varying beam step size (BSS) and Overdose/Undersize factor (ODUS)
- Characterization of the T-Gates show a very good lift-off and acceptable metal deposition





Design:
50 nm foot;
200 nm Wing

Design:
50 nm foot;
300 nm Wing

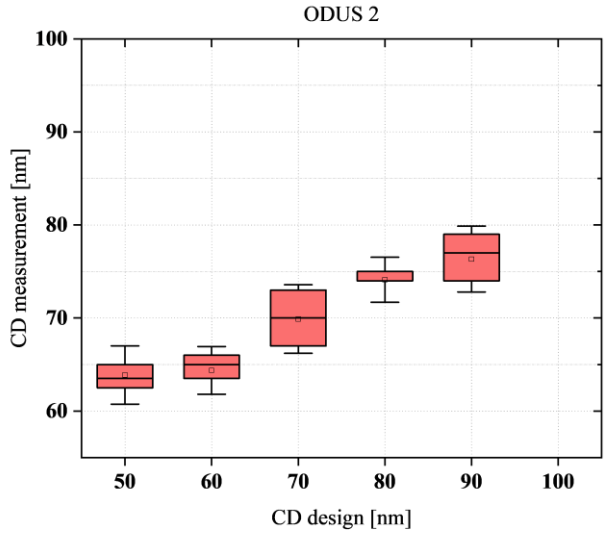
Design:
50 nm foot;
750 nm Wing

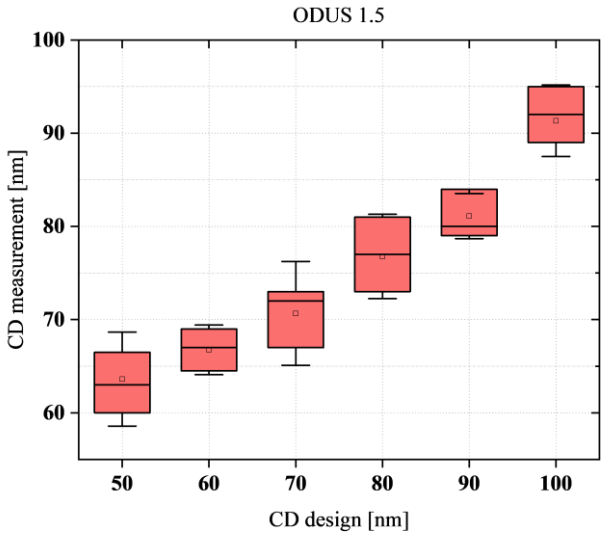
ODUS variation

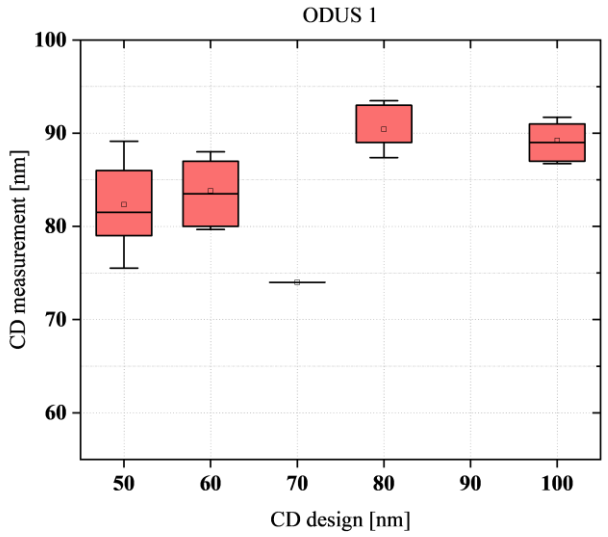
- Measurements of small foot design i.e. 20, 30 and 40 nm have great deviation of CD design
- Using ODUS causes improved structures and higher yield
- Increasing the ODUS factor elevates the stability of the T-Gates

→ High ODUS factor realizes superior, more stable T-Gates

	1	1.5	2
8 nm	-	-	+
10 nm	+	+	+
15 nm	-	-	+
20 nm	-	-	+



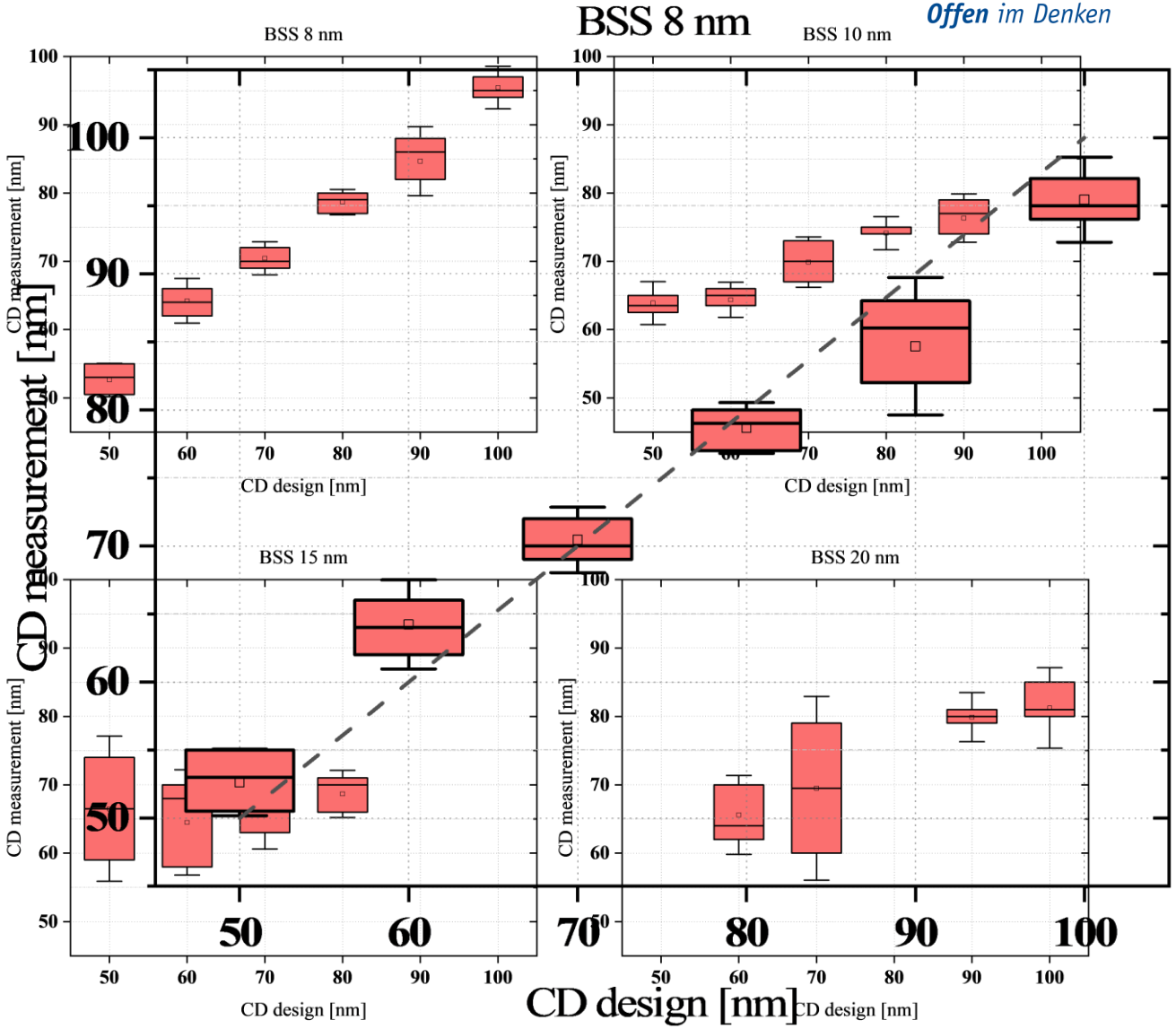




BSS variation

- Small BSS causes a multitude of improvements
- Reducing BSS shows an increase in yield
- Further reduction creates a linear dependency of CD measurement and CD design
- Minimizing BSS to 8 nm improves the linearity and heightens stability even more

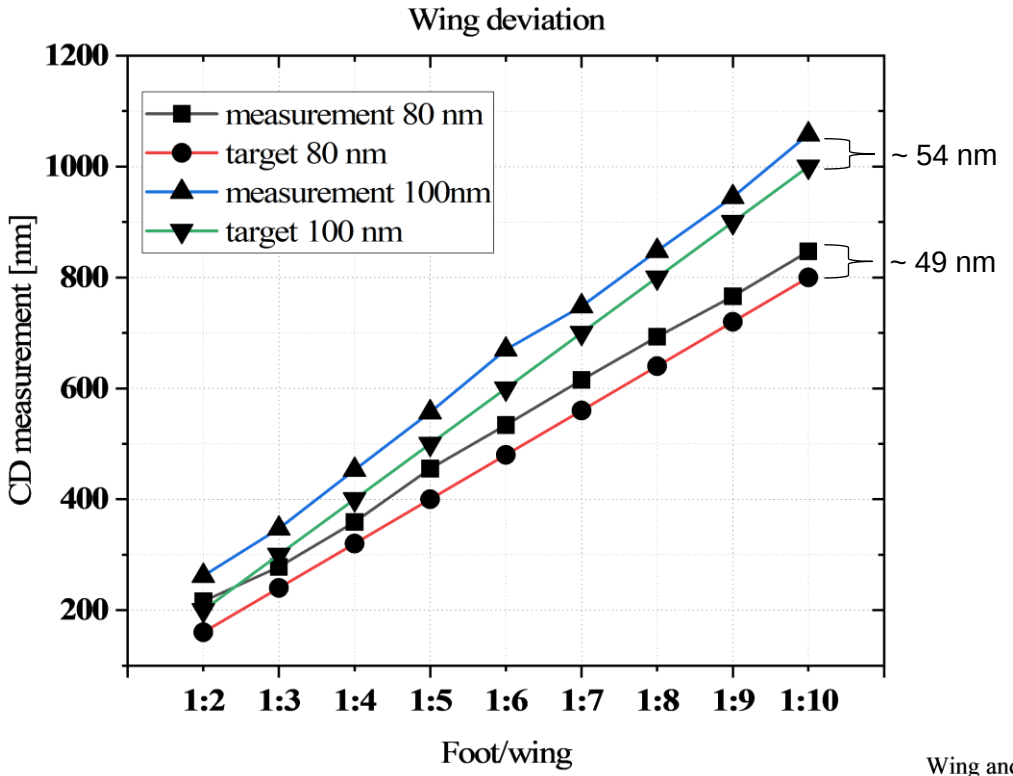
→ Low BSS with high ODUS factor delivers best results; and BSS 8 nm results in on-size foot-lengths with <10% deviation

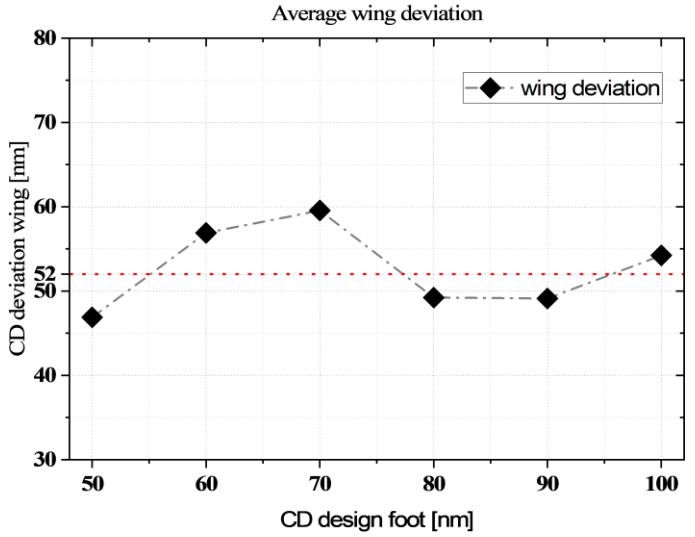


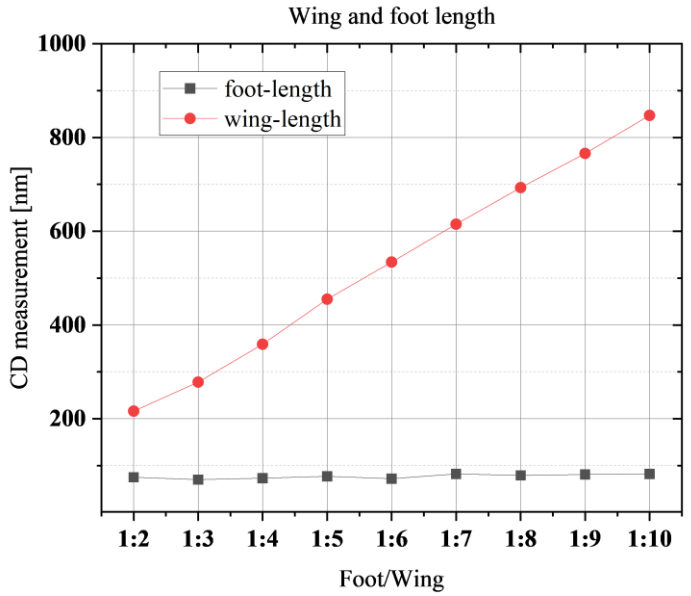
Wing dimensions

- Measurements of wing CD show deviation of designed CD
- Deviation is very similar on all foot/wing ratios and foot-lengths
- Fitted deviation around 52 nm
- Constant bias can counteract deviation in further processes
- Stable foot-lengths while wing-lengths increase

→ On size creation of wing possible, in up to 1:10 foot/wing ratio







Thank you very much! Are there any questions?

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References

- [1] S. Bentley, X. Li, D. Moran, and I. G. Thayne, "Two methods of realising 10 nm T-gate lithography," *Microelectronic Engineering*, vol. 86, 4-6, pp. 1067–1070, 2009, doi: 10.1016/j.mee.2008.12.029.
- [2] Y. CHEN, "Fabrication of ultra-short T gates by a two-step electron beam lithography process," *Microelectronic Engineering*, 73-74, pp. 662–665, 2004, doi: 10.1016/j.mee.2004.03.010.
- [3] D. J. Denninghoff, S. Dasgupta, J. Lu, S. Keller, and U. K. Mishra, "Design of High-Aspect-Ratio T-Gates on N-Polar GaN/AlGaN MIS-HEMTs for High $f_{\max}$," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 785–787, 2012, doi: 10.1109/LED.2012.2191134.
- [4] K. Karami *et al.*, "Robust sub-100 nm T-Gate fabrication process using multi-step development," *Micro and Nano Engineering*, vol. 19, p. 100211, 2023, doi: 10.1016/j.mne.2023.100211.
- [5] M. Zhu, Y. Xie, J. Shao, and Y. Chen, "Nanofabrications of T shape gates for high electron mobility transistors in microwaves and THz waves, a review," Micro and Nano Engineering, vol. 13, p. 100091, 2021, doi: 10.1016/j.mne.2021.100091.